EE2001 - Digital systems lab
Clocks, Flipflops and State machines

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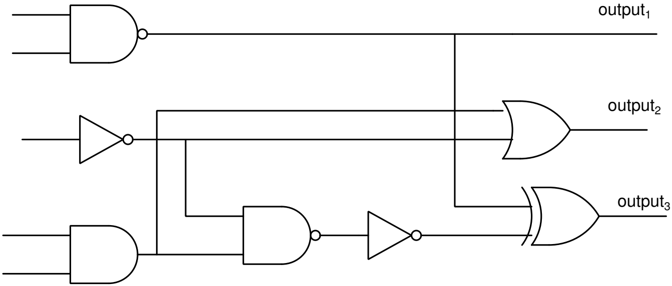
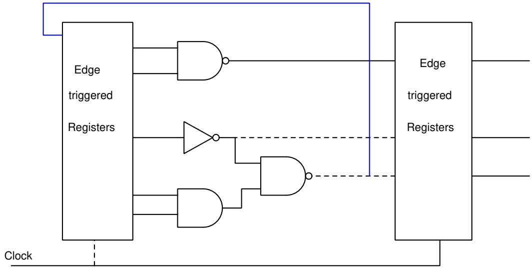
Why do we need flip-flops, registers?



- The arrival time for each output is different. It varies from IC to IC.
- As combinational circuits become larger, it becomes difficult/impossible to figure out when to check outputs.
- Use registers (flip flops) to store outputs and clocks to synchronize operations

Register transfer, State machines

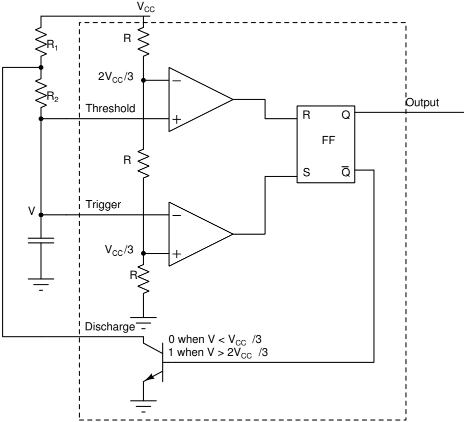


- Periodically store outputs using edge triggered flip-flops. Now we know outputs are available at clock edge.
- Clock frequency depends on the largest delay - delay of critical path. Estimate this delay and add some margin to get the clock period.
- Can also the feed the outputs back - State machine. Here, the "next state" of the register depends on the "present state"; Example - counters.

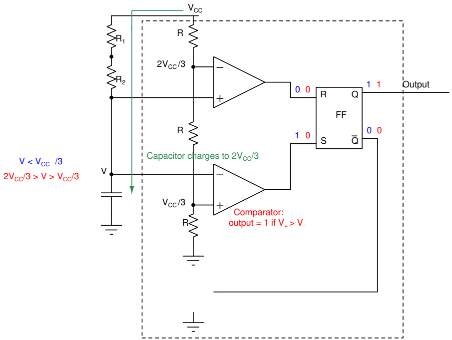
Clocks

- Crystal oscillators - Most accurate and stable
- Ring oscillators - Clock frequency variations large due to manufacturing variations
- Multivibrators based on RC time constants

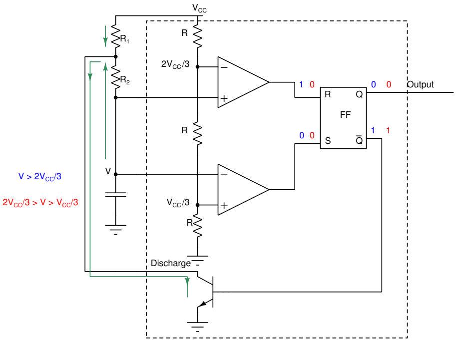
555 Timer



- When $V < \frac{V_{CC}}{3}$, S-R latch is set and output $Q = 1$
- When $V > \frac{2V_{CC}}{3}$, S-R latch is reset and output $Q = 0$. Since $\overline{Q} = 1$, the transistor is ON and the capacitor discharges.
- Charging time constant: $(R_1 + R_2)C$. Discharging time constant $= R_2C$

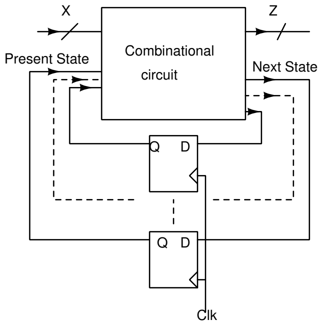


V_CC
R_1
R_2
R
2V_CC/3
R
V
V < V_CC /3
2V_CC/3 > V > V_CC/3
Capacitor charges to 2V_CC/3
V_CC/3
R
Comparator:
output = 1 if V+ > V-
0 0
1 0
1 1
0 0
R
Q
FF
S
Q̄
Output



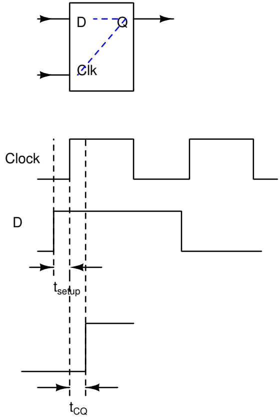
V_CC
R_1
R_2
R
2V_CC/3
R
V
V > 2V_CC/3
2V_CC/3 > V > V_CC/3
V_CC/3
R
Discharge
1 0
0 0
0 0
1 1
R
Q
FF
S
Q̄
Output

State Machines: Modelling using Verilog




```
module StateMach( X, Z, clock );

input X ;
input clock;
output Z;
reg PresentState;
wire NextState;

 always@(posedge clock)
begin
PresentState = NextState
end

assign Z = X & PresentState;

assign NextState = X | PresentState;

endmodule
```

Propagation delays of a (edge triggered) Flipflop



- Setup time: The time for which the data should be stable before arrival of the clock edge.
- Clock-to-Q delay: The last input to arrive should be the clock. The delay between the arrival of the clock edge and the output transition is the propagation delay.

Experiment 9

Objective: Model and build Sequential circuits

- Realize a 1kHz oscillator using the 555 timer. Use both channels of the oscilloscope to display the capacitor and output voltage. How will you achieve a duty cycle of nearly 50% with the 555? The minimum R_1 should be about $1k\Omega$, so that the capacitor is able to discharge through the transistor.
- Using 3 bits of the 4 bit counter (74163) and parallel load, construct a mod-5 counter that counts from 0,1,2,3,4 and back to 0.
- Design a 4 bit ripple counter using J-K Flipflops. Estimate the propagation delay of the flip-flop. If measurement is difficult, increase the number of bits.

- Design a sequential circuit with two D flip flops A and B and one input x_{in}. When $x_{in} = 0$, the state of the circuit remains the same. When $x_{in} = 1$, the circuit goes through the state transitions from 00, 01, 11, 10 and back to 00 and repeats. (a) Model and simulate the statemachine using Verilog. (b) Wire and test it on breadboard.