A Micropower Log-Domain Filter Using Enhanced Lateral PNPs in a 0.25 μm CMOS Process

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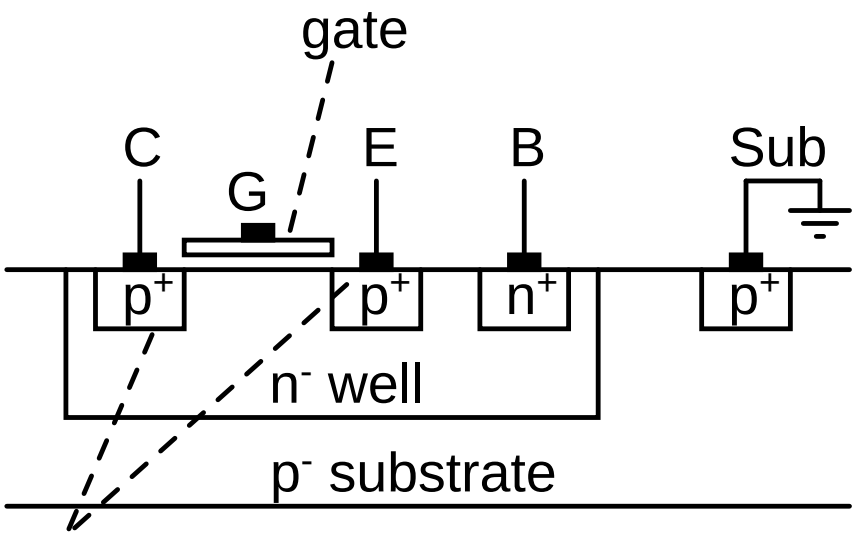
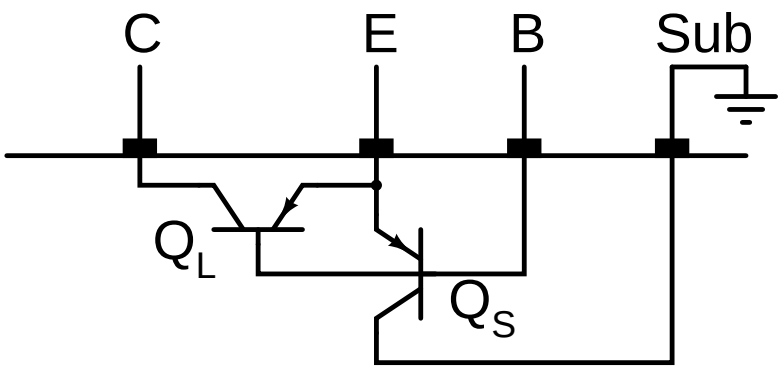
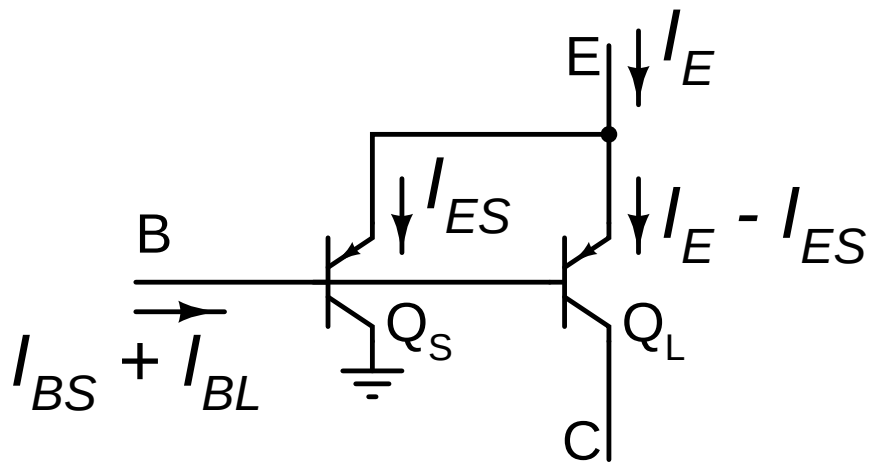
Outline

- Enhanced lateral PNP transistor.
- Log-domain filter.
- Measurement results.
- Conclusions.

Conventional lateral transistor

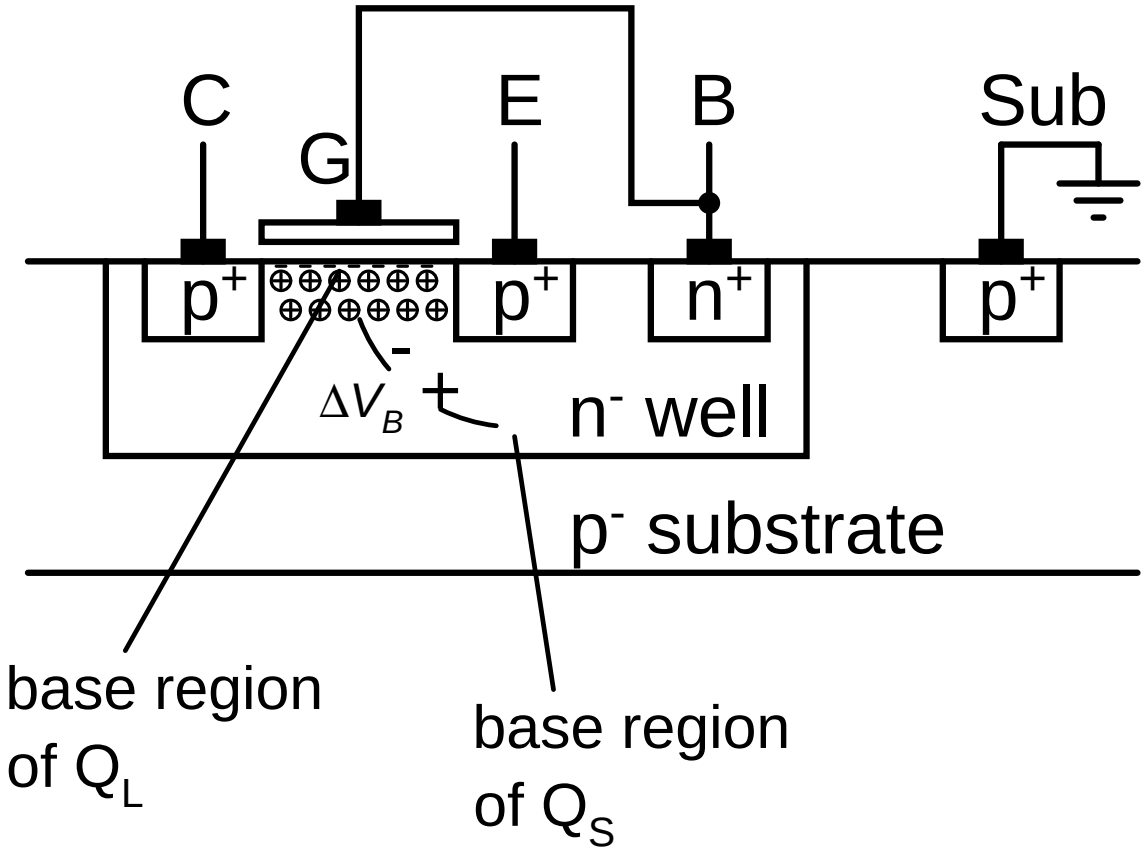






- Parasitic transistor Q_S lowers α and β.

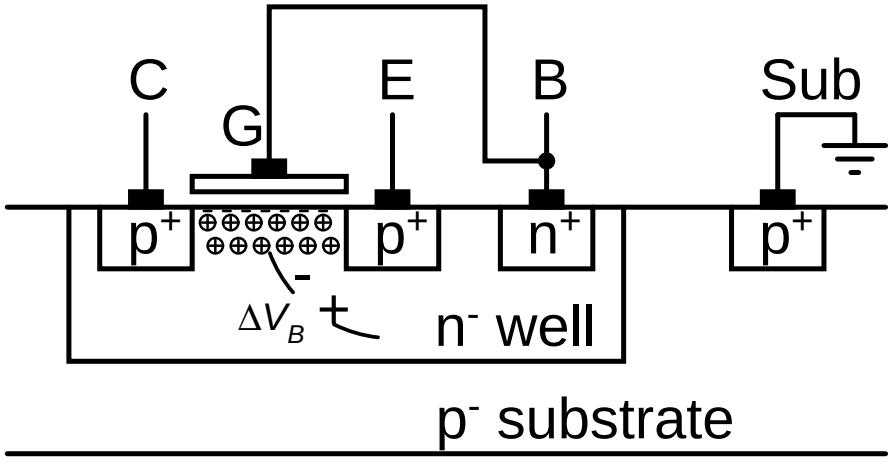
Enhanced lateral transistor

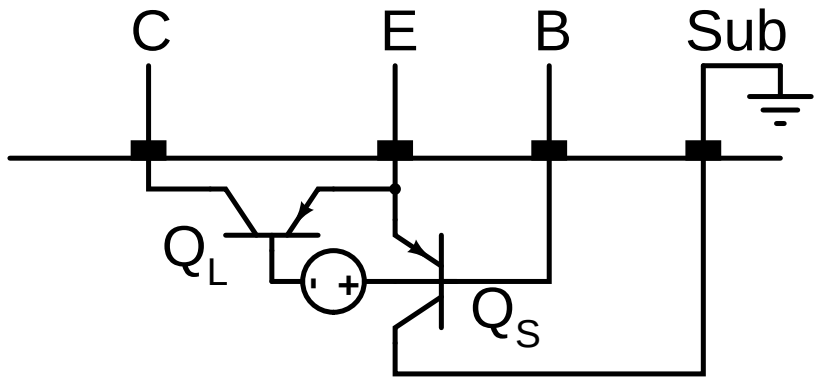


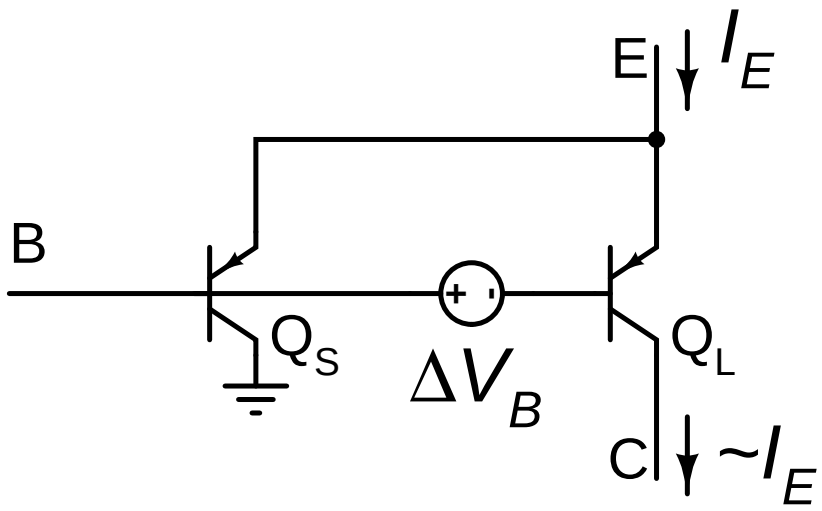
[Verdonckt-Vandebroek, ’91]

- Gate connected to the base.
- Surface is more negative than deep inside the n^- well.

Enhanced lateral transistor

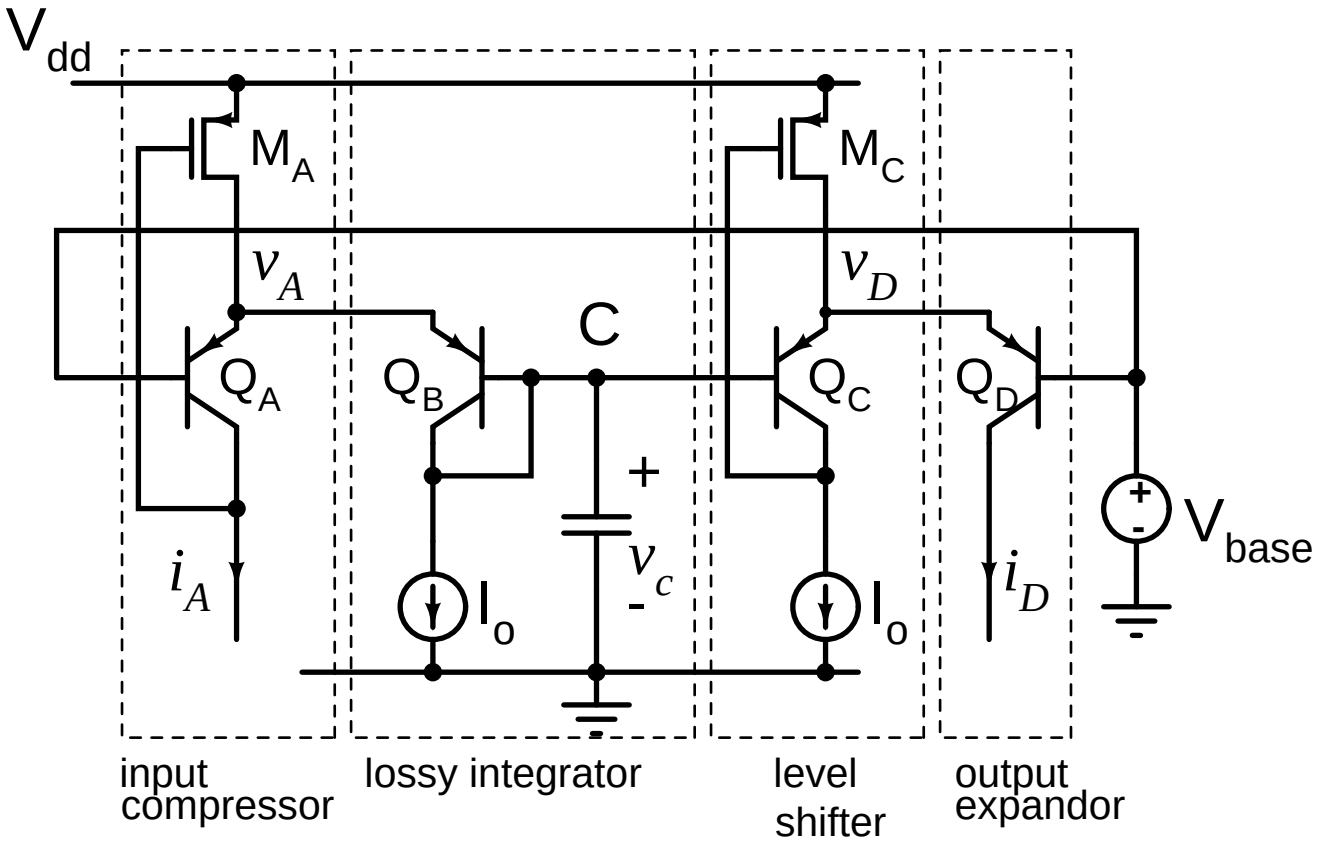






- $V_{EB}(Q_S) < V_{EB}(Q_L) \Rightarrow Q_S$ is suppressed.

First-order log-domain filter

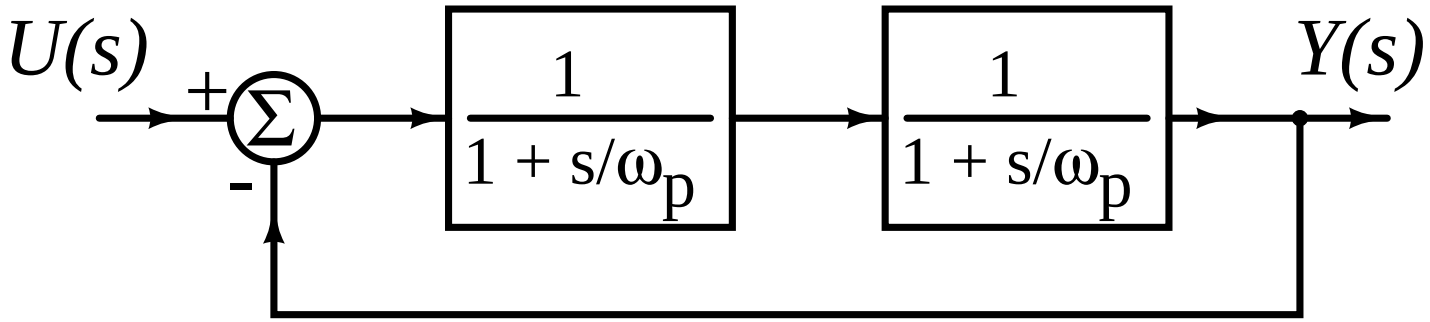


[Punzenberger '97]

$$\frac{di_D}{dt} = -\frac{I_0}{CV_t} i_D + \frac{I_0}{CV_t} i_A$$

- Large signal linear from i_A to i_D.

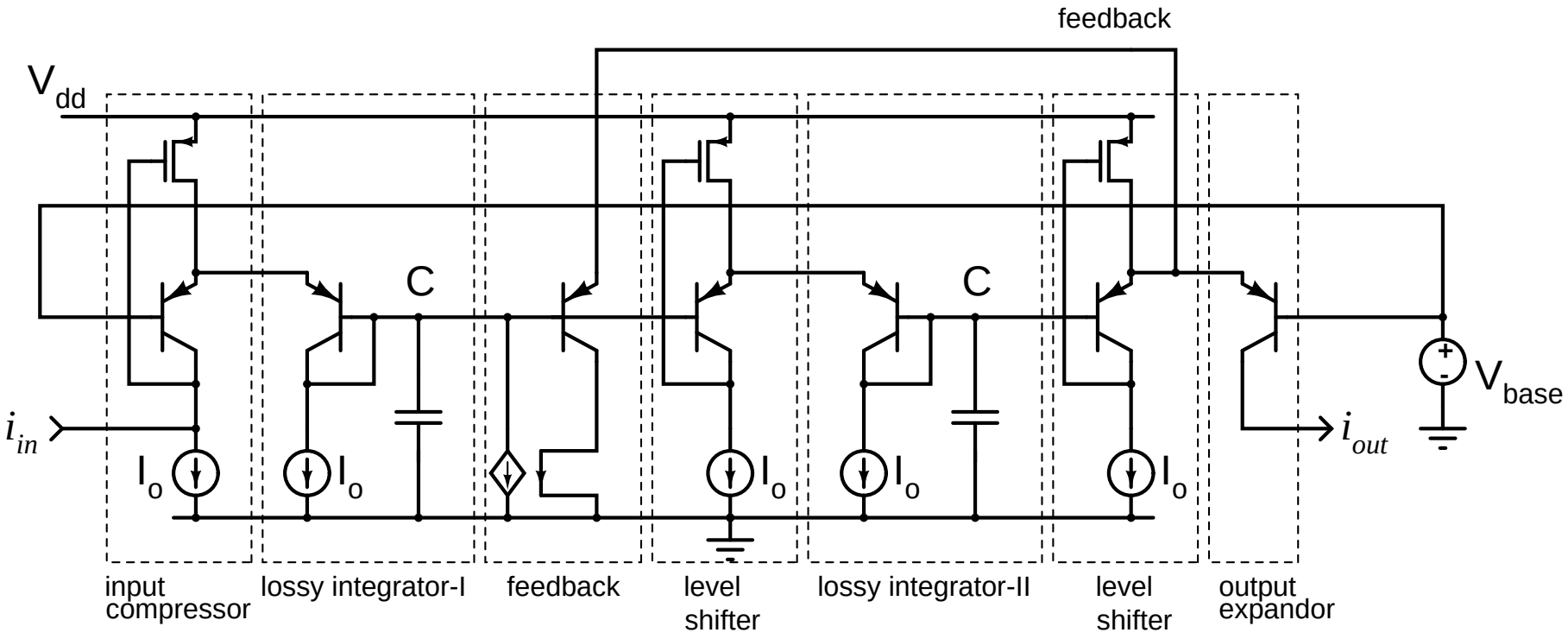
Second-order Butterworth filter



$$\frac{Y(s)}{U(s)} = \frac{1/2}{1 + (s/\omega_p) + (s/\sqrt{2}\omega_p)^2}$$

- Two first-order filters in a feedback loop.

Second-order Butterworth filter

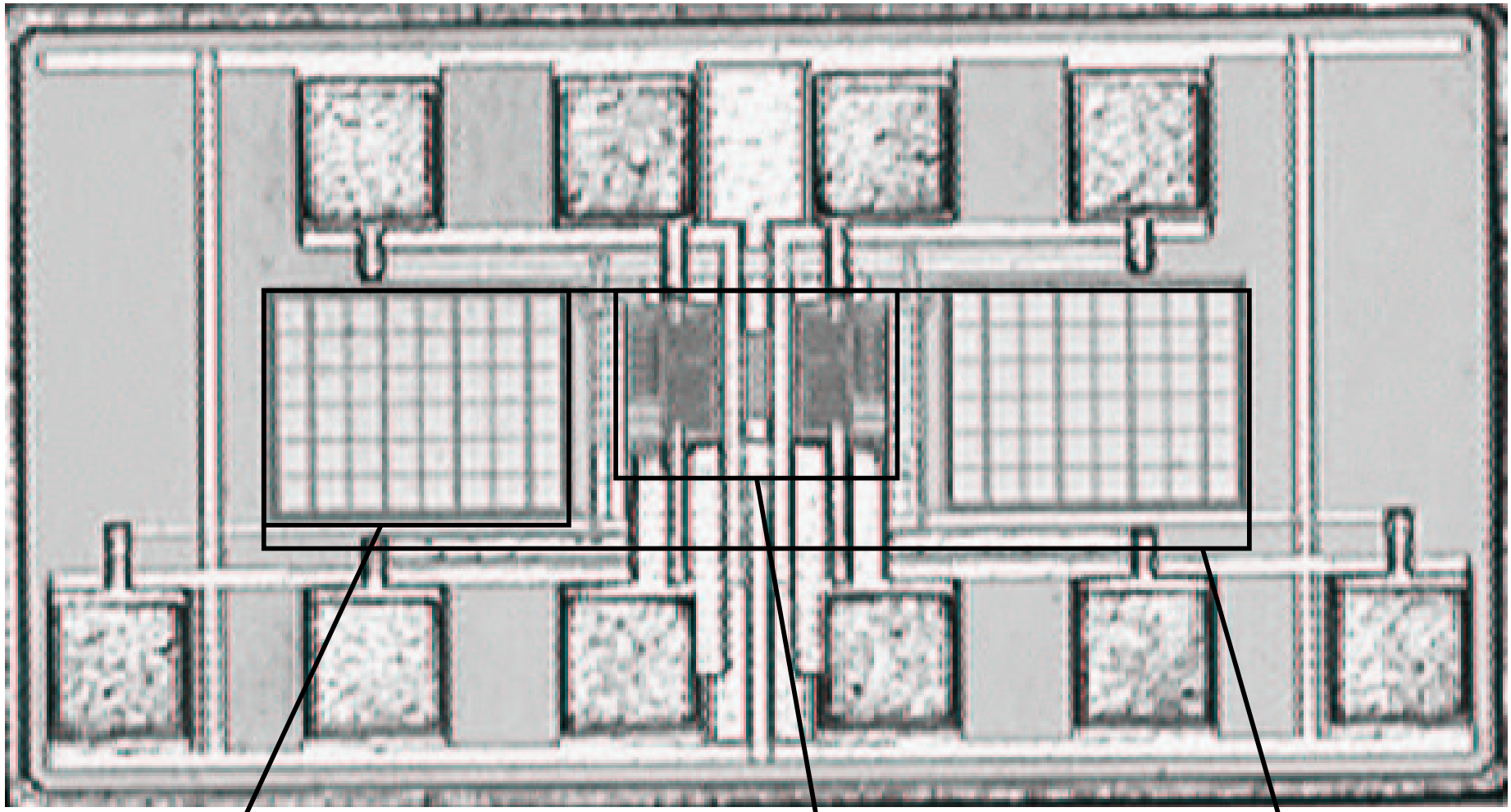


- bandwidth = $\sqrt{2}I_0/C$ rad/s.

Second-order Butterworth filter

- 0.25 μm CMOS technology.
- Enhanced lateral PNP transistors.
- pMOS accumulation capacitors.
- Supply voltage = 1.5 V.
- $I_0 = 0.5\,\mu$A.

Chip photograph

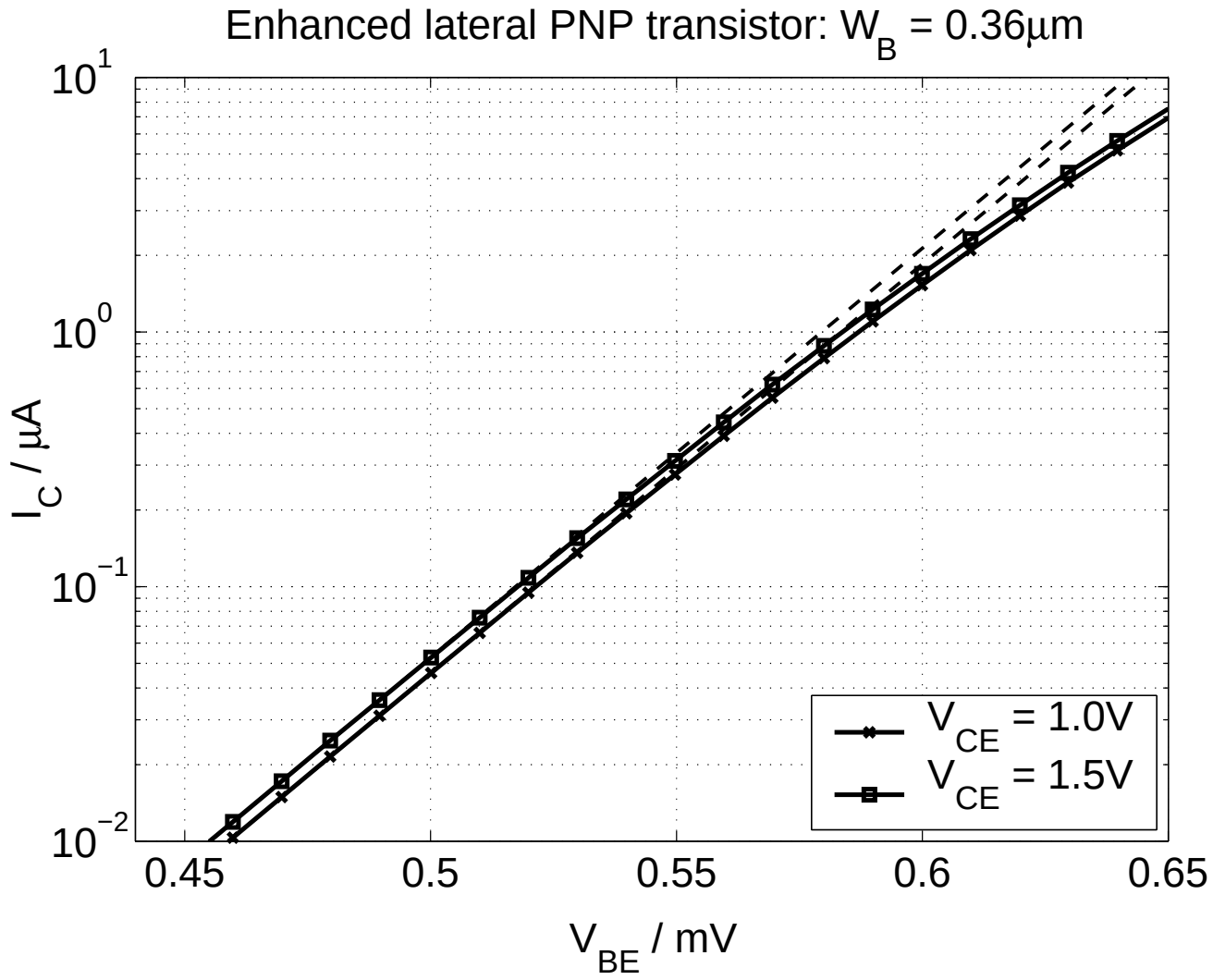


pMOS accumulation capacitor (0.022 mm^2)

active circuit

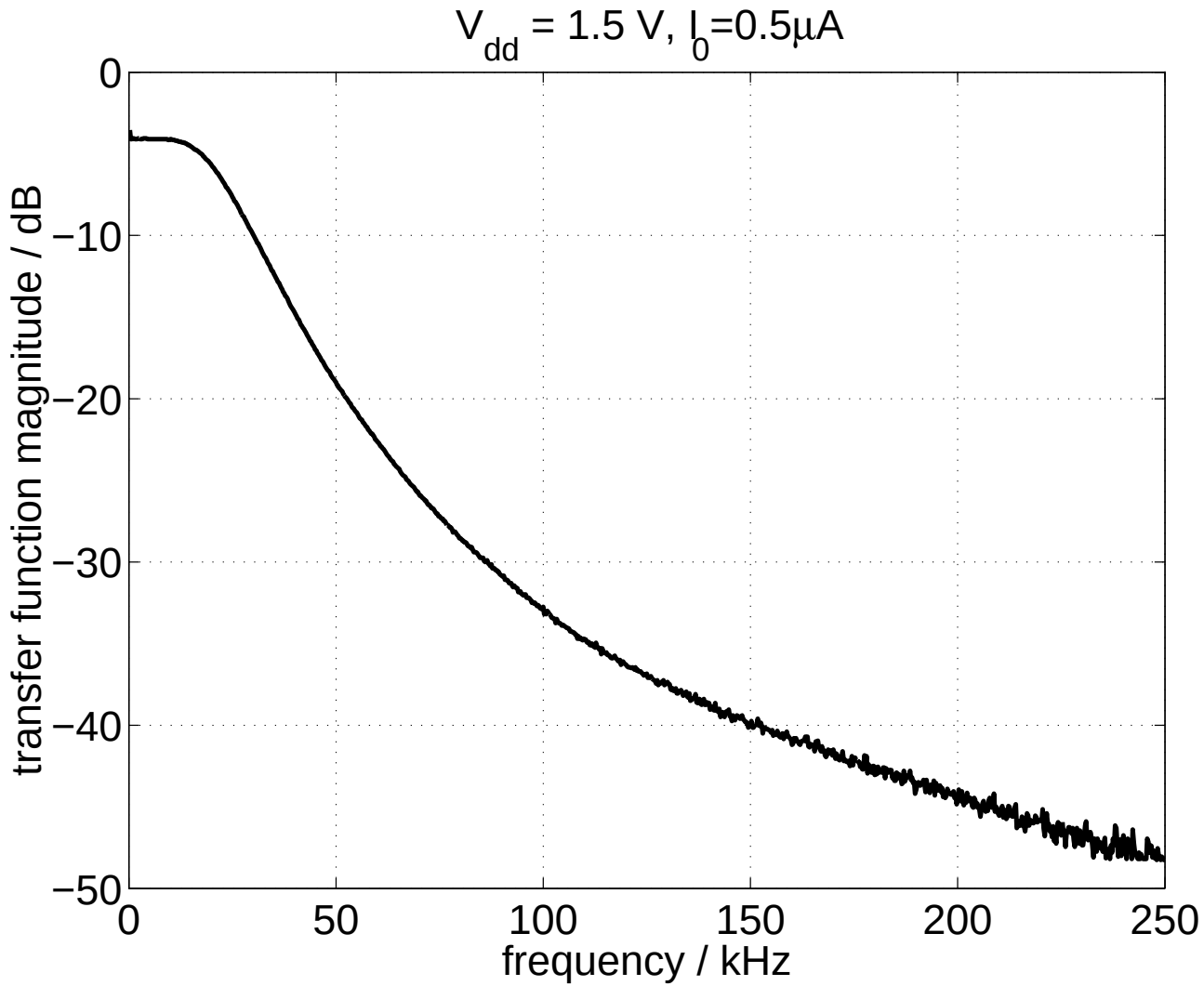
0.085 mm^2

Lateral PNP: Measured I-V characteristics



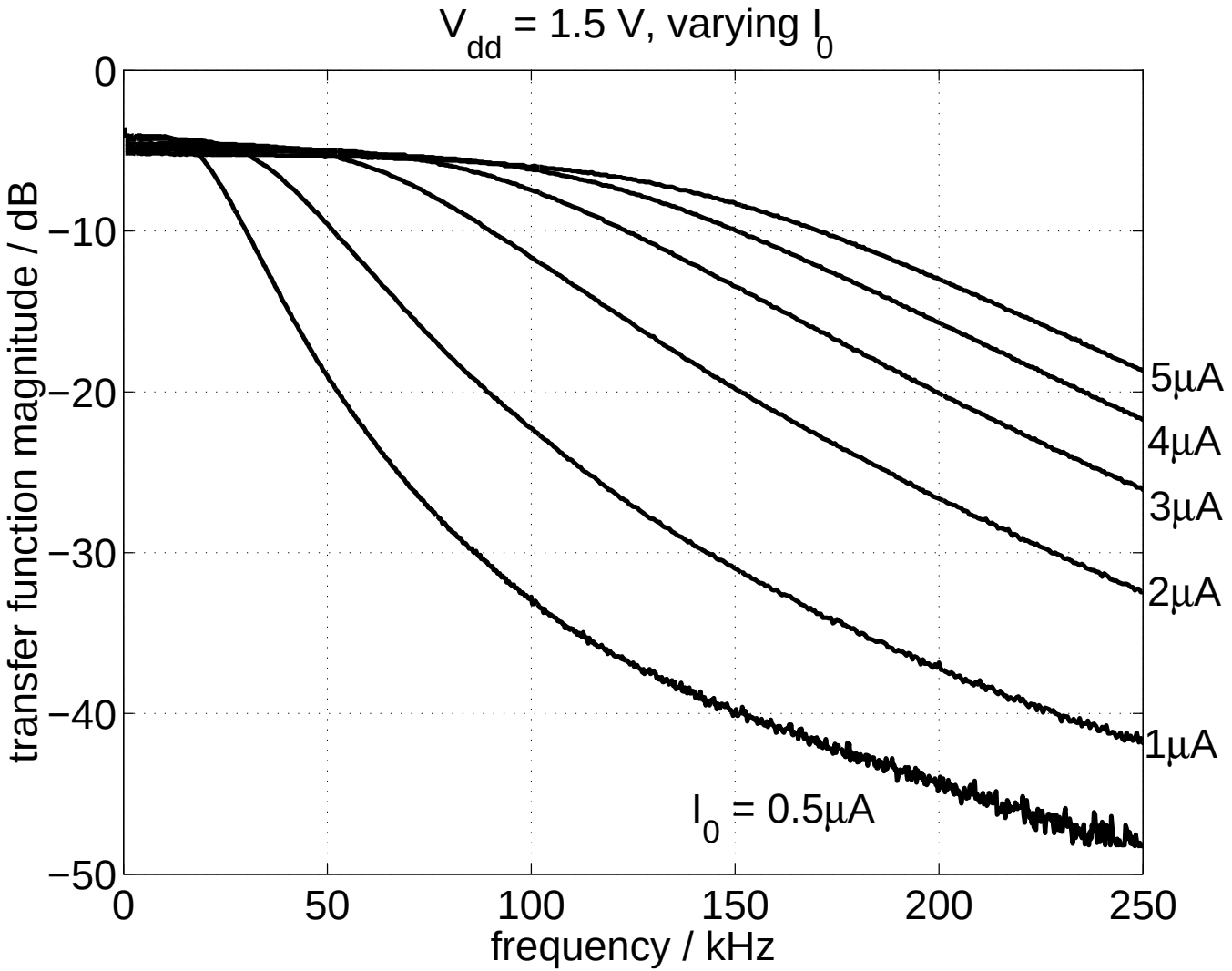
- Slope factor = 1.04; Early voltage = 2.3 V.

Measured results: Frequency response

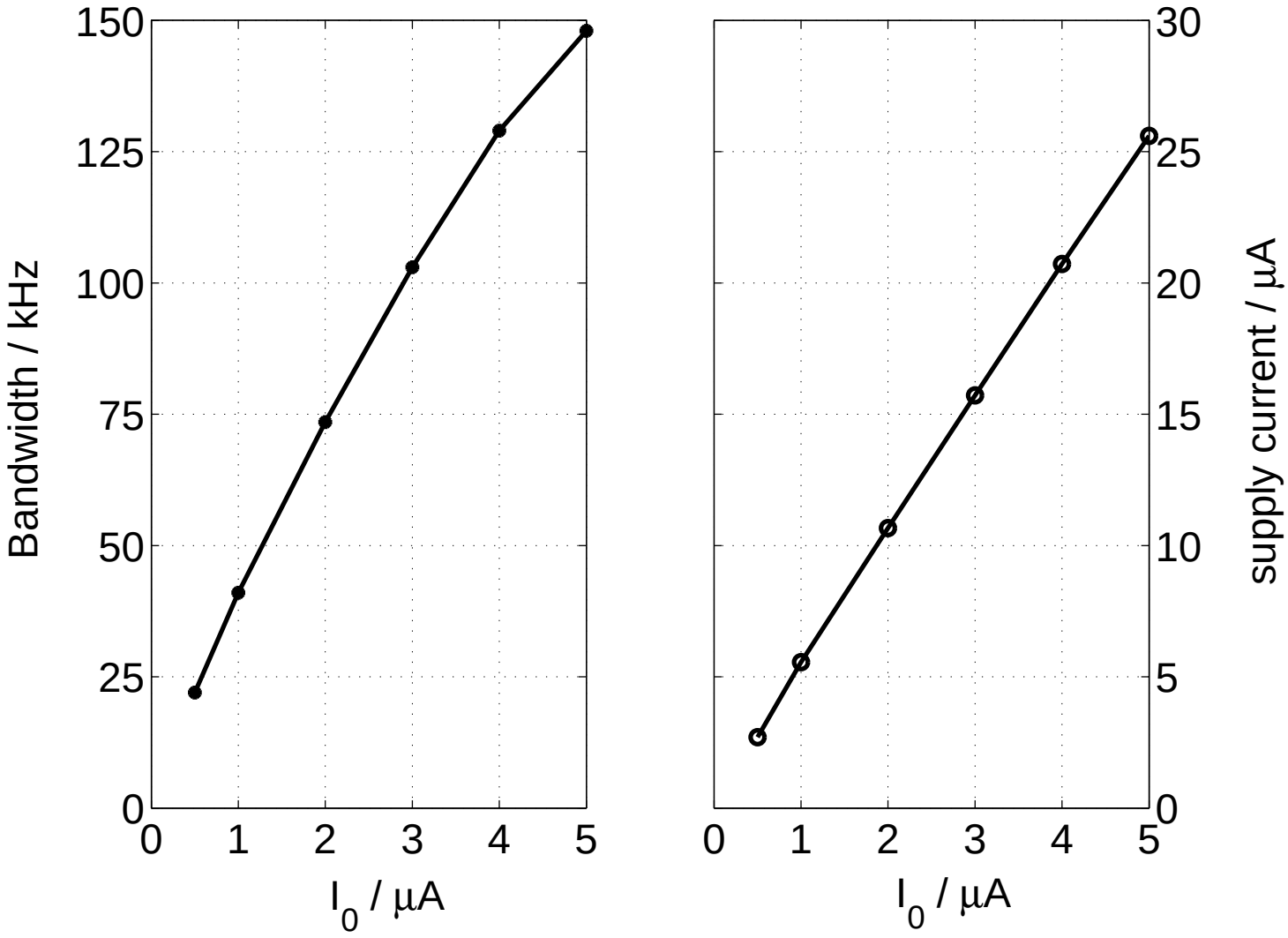


- dc gain = -4.1 dB; bandwidth = 22 kHz.

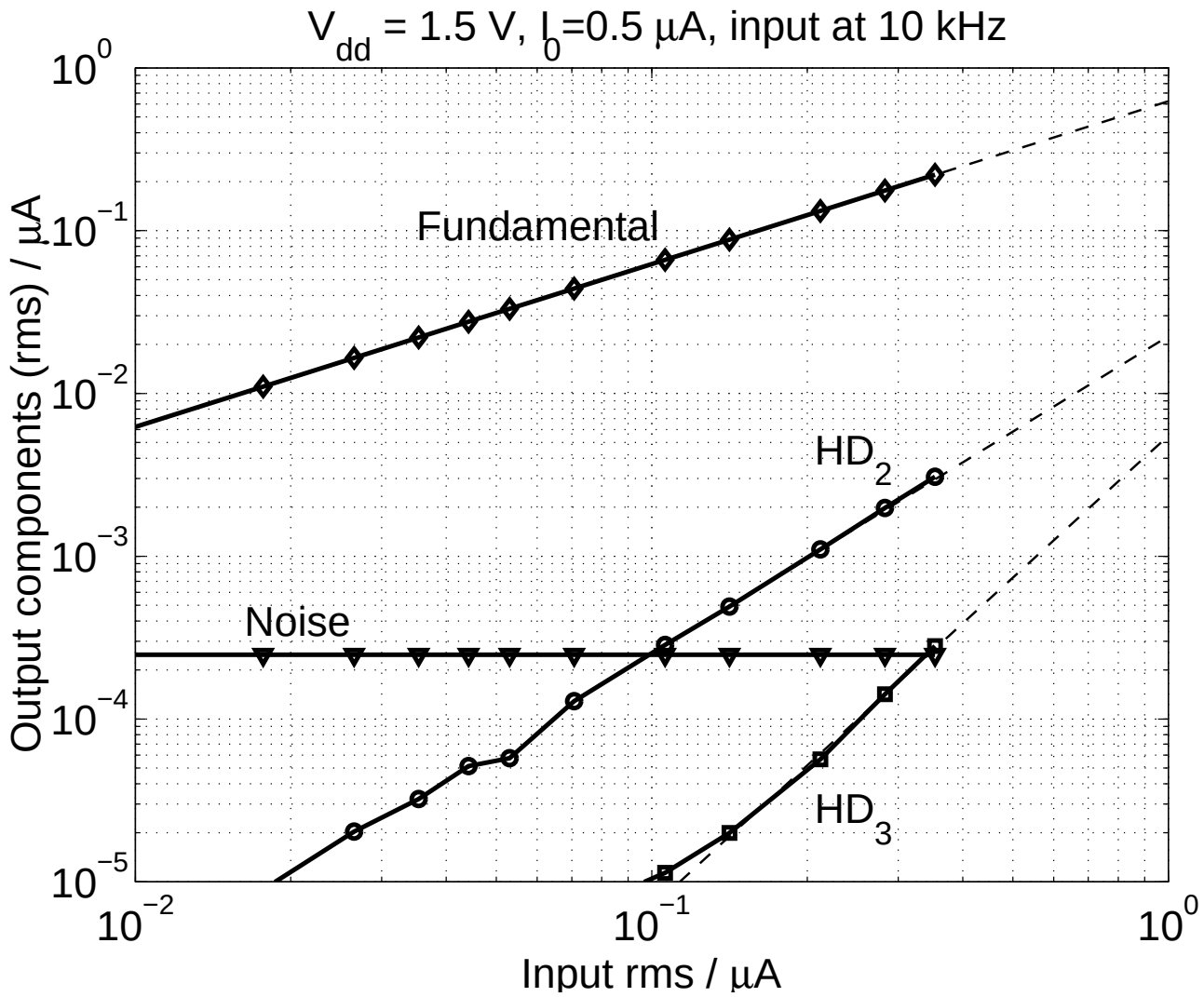
Measured results: Tuning



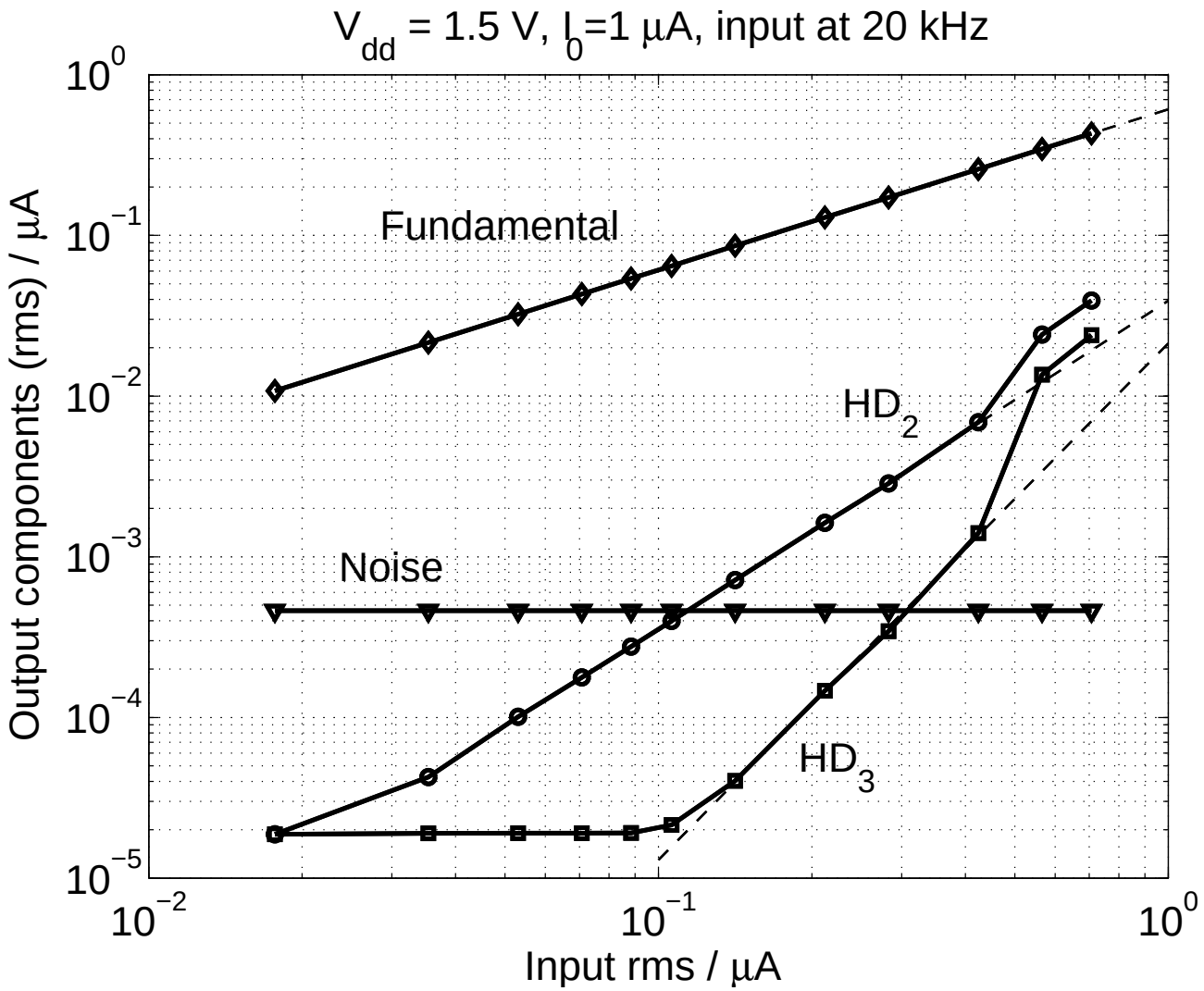
Bandwidth and current consumption



Measured results with $I_o = 0.5\,\mu$A



Measured results with $I_o = 1\,\mu$A



Summary

Technology	0.25 μm CMOS	
Chip area	0.085 mm^2 (excl. pads)	
Supply voltage	1.5 V	
Bias current (I_0)	$0.5\mu A$	$1\mu A$
-3 dB BW (kHz)	22	41
Power diss. (μW)	4.1	8.3
o/p noise (rms nA)	0.25	0.46
S/N @ 1 % THD	56.1 dB	47.0 dB
Max. $S/(N+THD)$	44.9 dB	40.5 dB
$\frac{\text{Power dissipation}}{\text{order}\cdot\text{BW}}$	93.2 pJ	101.2 pJ

Conclusions

- An alternative technique for designing log-domain filters in CMOS technologies is explored.
- A second-order filter using enhanced lateral PNP transistors is demonstrated.
- Performance of the prototype filter is shown to be comparable to that of log-domain filters fabricated in bipolar technologies.