A 100 μW Decimator for a 16 bit 24 kHz bandwidth Audio $\Delta\Sigma$ Modulator

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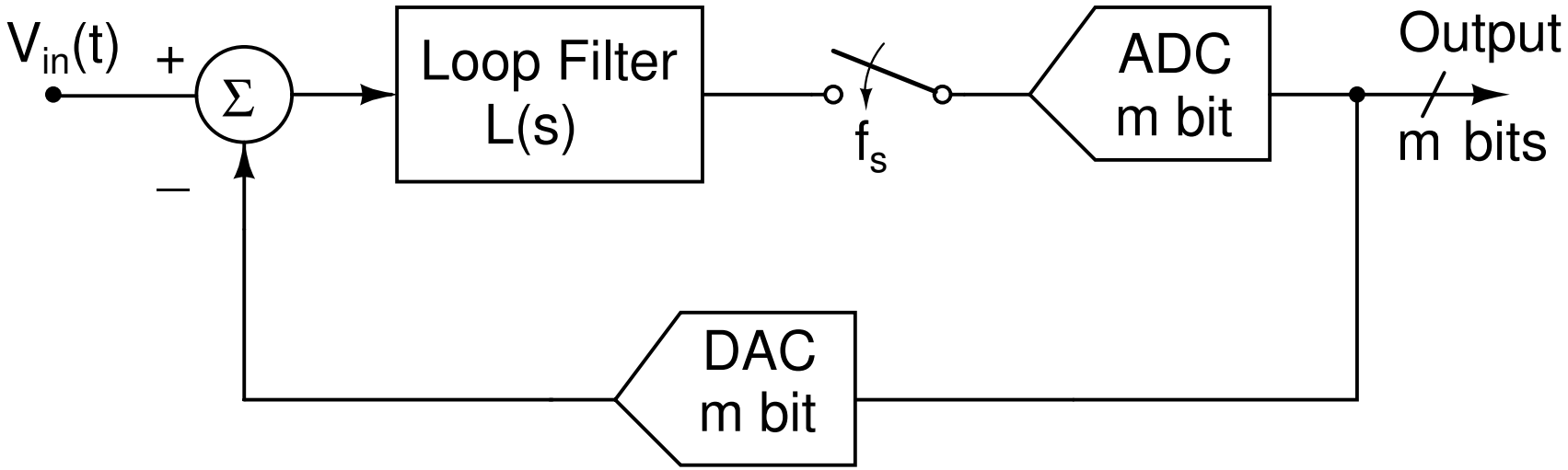
Outline

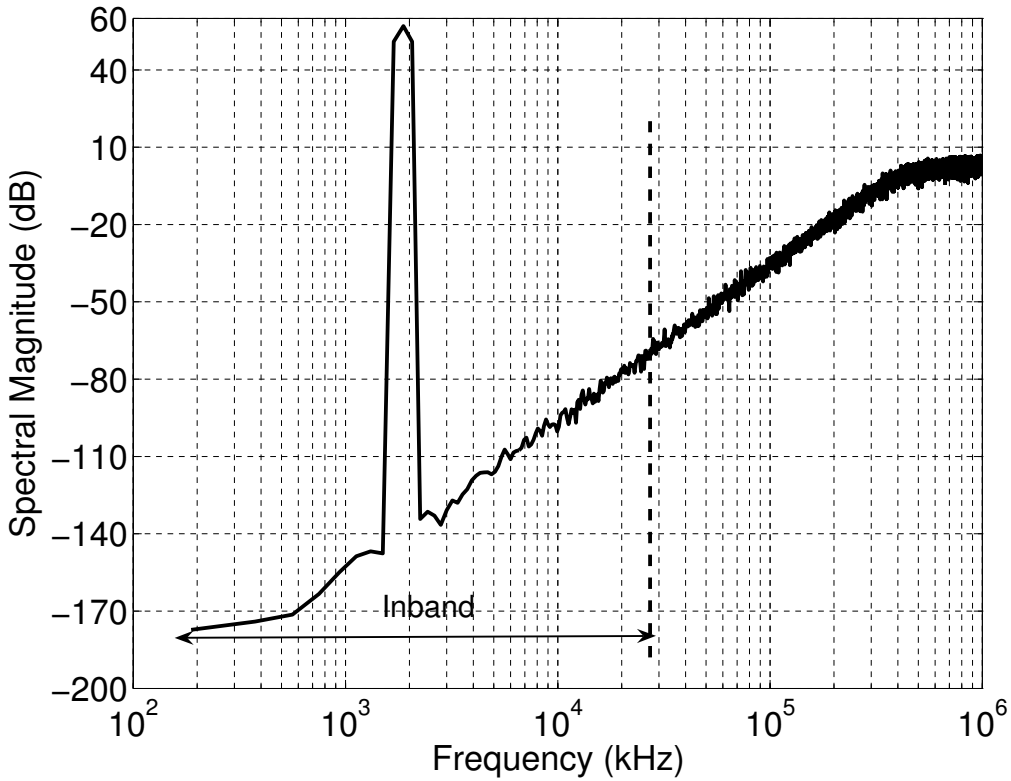
- Brief overview of $\Delta\Sigma$ Modulators & Decimators
- Architectural optimizations in decimator to reduce power
- Simulation results
- Fabricated chip results
- Conclusions

Block diagram - Continuous Time ΔΣ Modulator



- Oversampling
- Noise shaping
- Low resolution internal ADC

Spectrum of the ΔΣ Modulator output



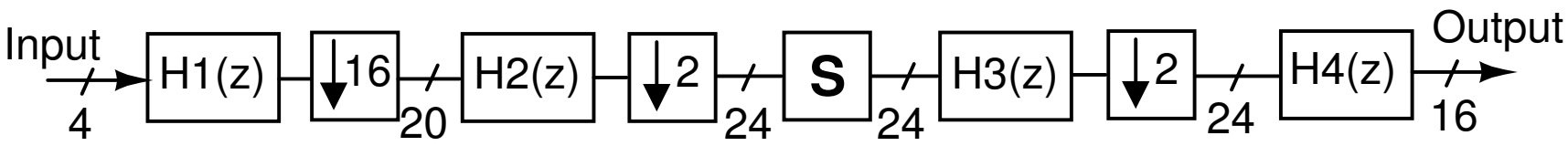
- 3^{rd} order L(s) , 4 bit ADC, f_s = 3.072 MHz
- Inband Signal to noise ratio (SNR) = 96 dB
- Decimator - Low pass filtering & downsampling

Decimator requirements

Modulator[1]		**Decimation Filter**	
Order	3	Downsampling Factor	64
Sampling rate	3.072 MHz	Passband ripple	0.05 dB
Nyquist rate	48 kHz	Passband edge	21.6 kHz
SNR	93 dB	SNR	96 dB
Power	90 μW	Power	$<$ 100 μW

[1] - S. Pavan, N. Krishnapura, R. Pandarinathan, and P. Sankar, "A power optimized continuous-time $\Delta\Sigma$ converter for audio applications," *IEEE Journal of Solid-State Circuits,* vol. 43, no. 2, pp. 351 360, 2008

Block diagram of the decimator



H1(z): SINC4

H2(z): First Halfband filter

H3(z): Second Halfband filter

H4(z): Equalizer

S : Scaling block

- Multistage decimation

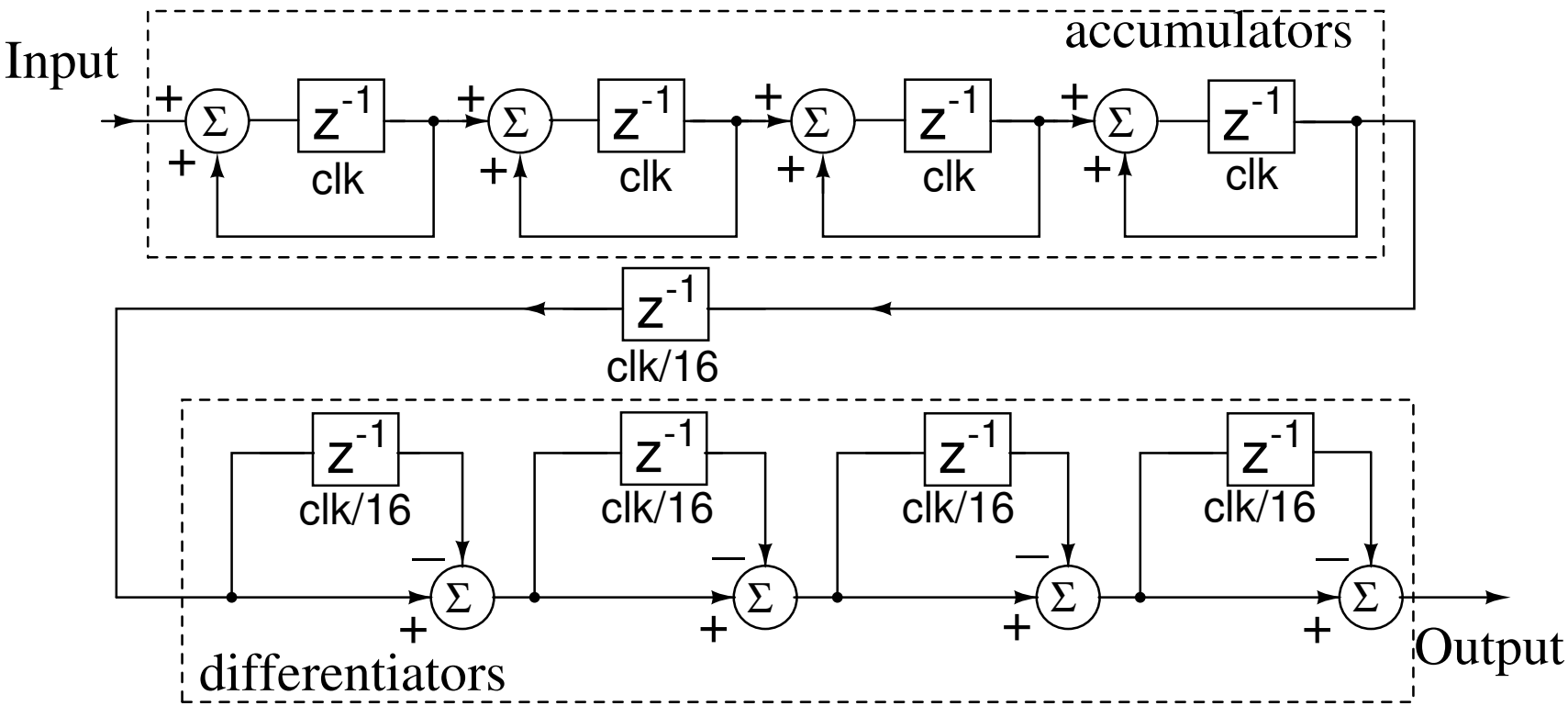
SINC4 filter

- SINC, $H(z)$ - 16 tap moving average filter
- SINC4, $H^4(z)$ - Cascade of 4 SINC filters
- Removes quantization noise shaping
- Downsampling of 16 - Hogenauer structure

$$H(z) = \frac{1 - z^{-16}}{1 - z^{-1}}$$

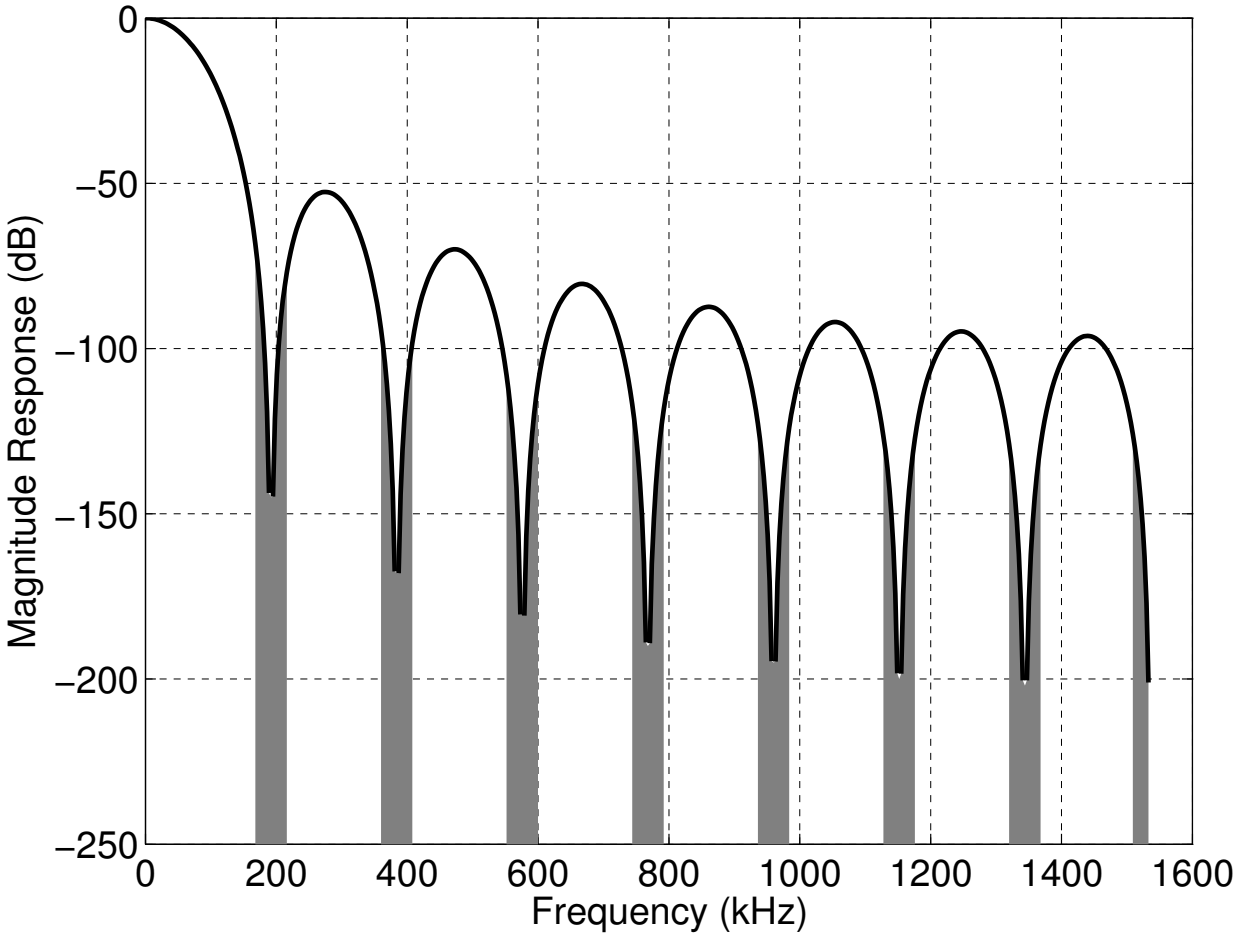
$$H(f) = \frac{sin(16\pi f)}{sin(\pi f)}$$

SINC4 - Hogenauer structure



- Retiming, Pipelining save 46% power in SINC4
- Optimal Datawidth = $B_{in} + k \log_2 N = 20$

Frequency response of SINC4



Shaded Area - Noise aliasing bands

Halfband filters

- FIR filters
  - 6 dB bandwidth = $\frac{f_s}{4}$
  - Alternate tap weights are 0
- Two halfband filters downsample by 2 each
- First halfband filter
  - Initial filtering
  - 10^{th} order
- Second halfband filter
  - Sharper filtering
  - 50^{th} order

Halfband filter implementation

- Polyphase structure, downsampling by 2 within filter
- Tap weights in Canonical Signed Digits (CSD)

$$\text{Example: } 0.875 = 2^{-1} + 2^{-2} + 2^{-3} = 2^{0} - 2^{-4}$$

(Reduces Multiplication Complexity)

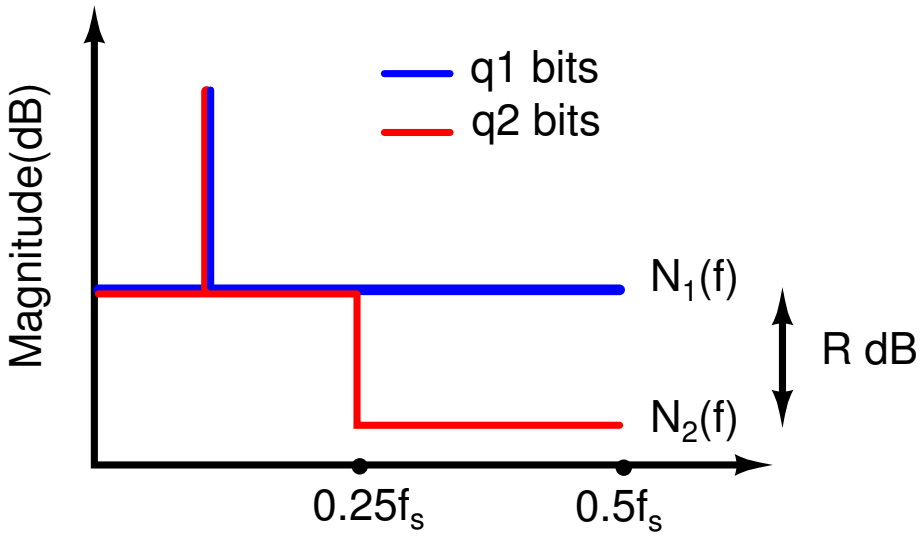
- Nested Multiplication, Horners rule

$$\text{Example: } 2^{-5} - 2^{-7} = 2^{-5}(1 - 2^{-2})$$

(Reduces Truncation Error)

- 2^{-1} is dropping a bit in the multiplicand

Datawidth in halfband filters



$$N_1(f) = 10^{\frac{-6q_1}{10}}$$

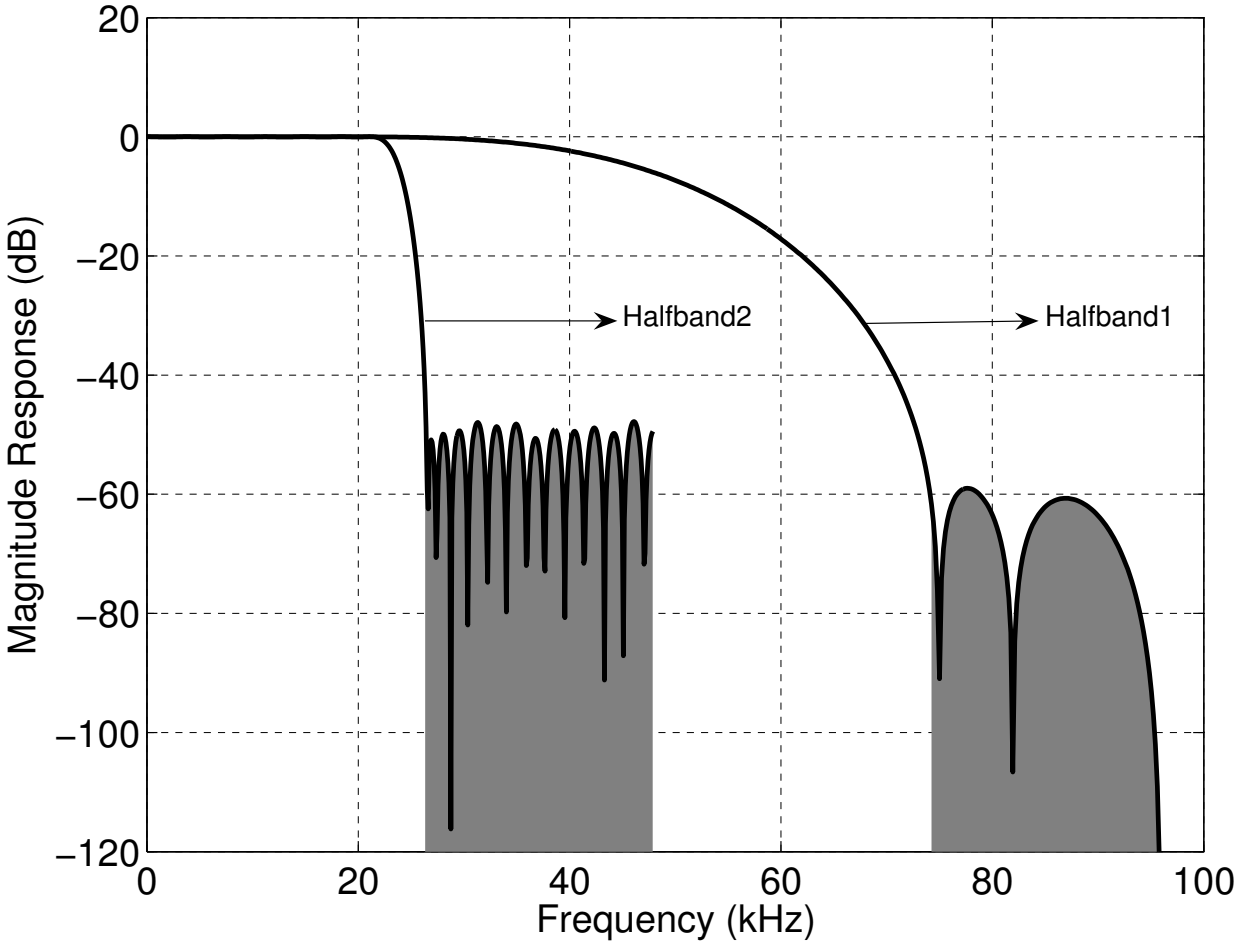
$$N_2(f) = 10^{\frac{-6q_2}{10}}$$

$$R = 10\log\frac{N_2}{N_1}$$

$$q_2 = q_1 + \frac{R}{6}$$

To attenuate a portion of quantization noise floor of a q_1=16 bit signal by 48 dB in some band needs q_2=24 bit in the filter.

Frequency response of halfband filters



Shaded Area - Noise aliasing bands

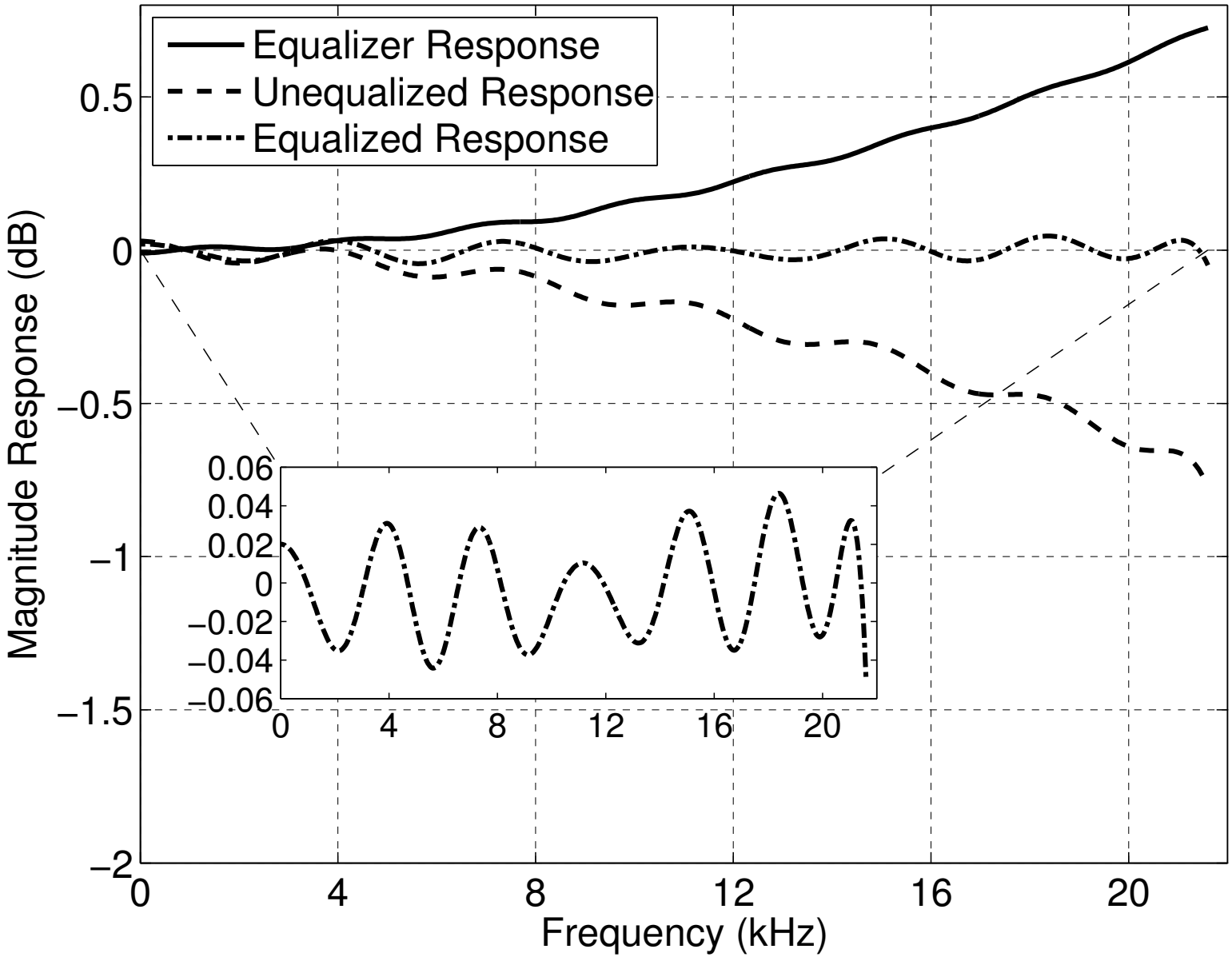
Scaling block

- $\Delta\Sigma$ Modulator - Maximum Stable Amplitude (MSA=85%)
- Signal swing at modulator output is MSA $\times$ fullscale
- 96 dB SNR at Nyquist rate only with fullscale amplitude
- Scale by MSA^{-1} after first halfband filter
- Lesser number of bits from modulator (4) and high frequency noise prevents scaling at the initial stages of decimator
- CSD & Nested Multiplication

Equalizer

- Droop of SINC4 in the passband
- Maximum passband ripple = 0.05 dB
- Inverse SINC4 designed with *Parks McClellan* method
- 48^{th} order filter
- CSD & Nested Multiplication

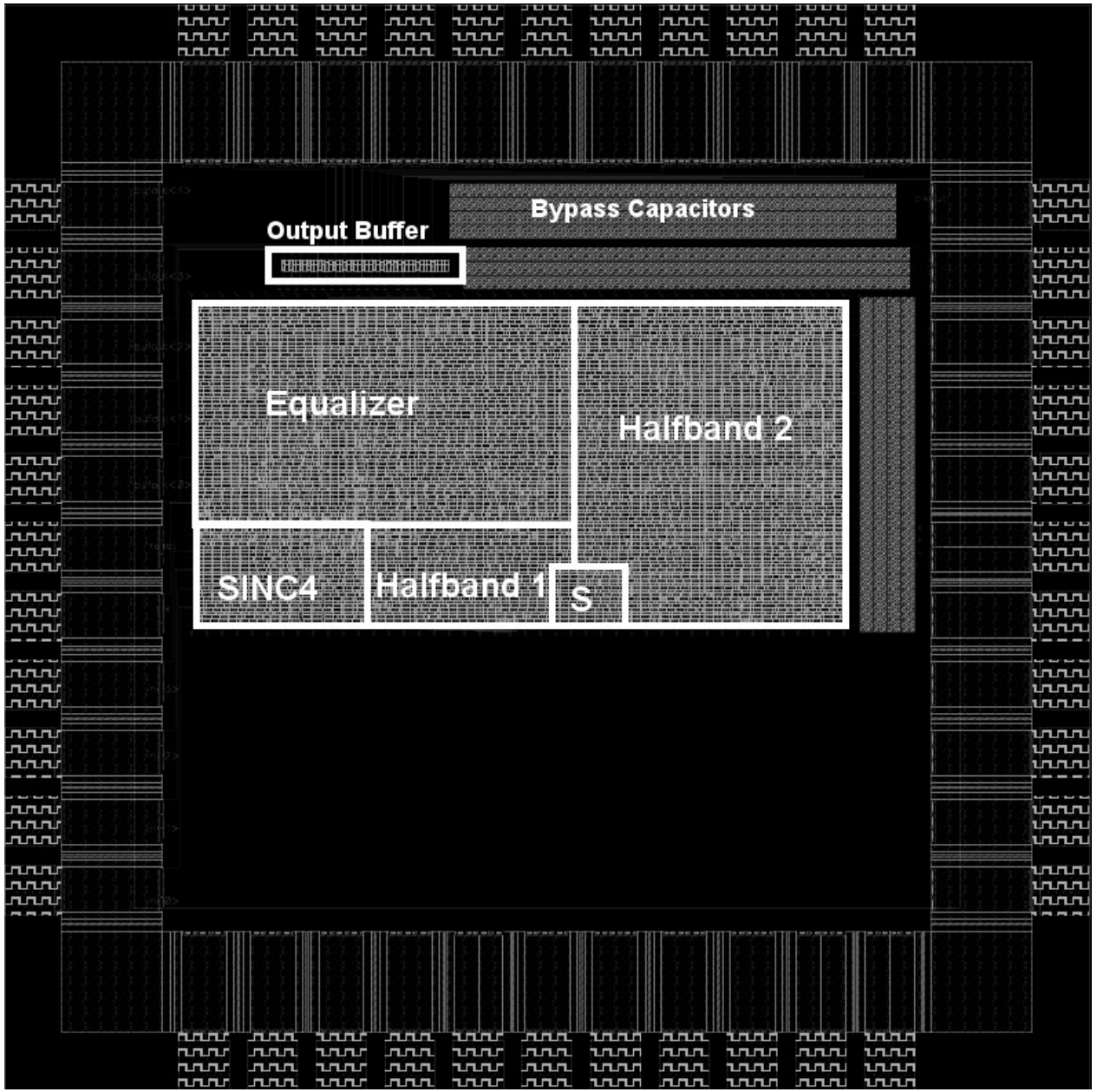
Frequency response of the equalizer



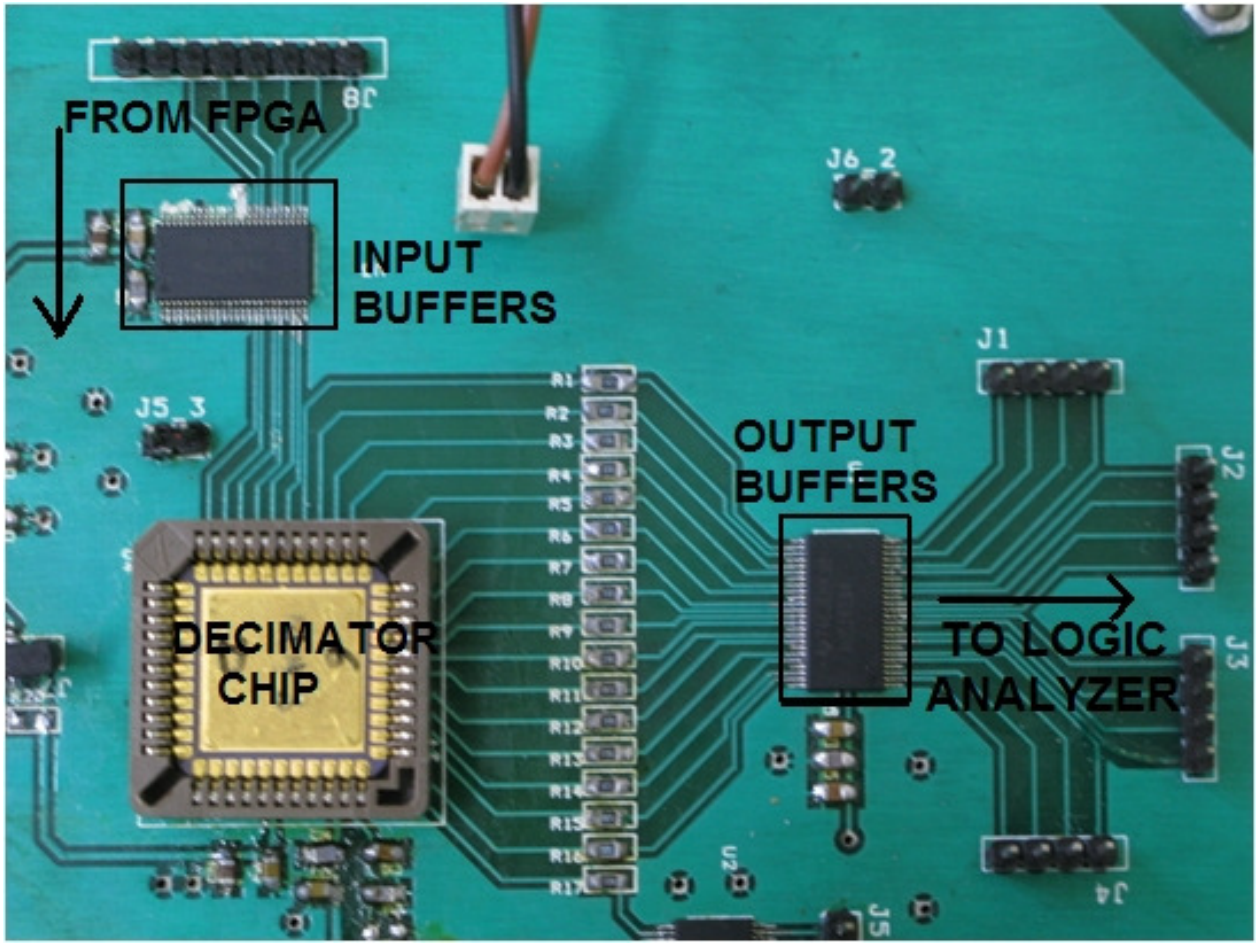
Synthesis

- Technology: 1.8 V standard cells UMC 0.18 μm CMOS
- CAD tools
  - Design Synthesis - Design Compiler
  - Place & Route - SoC Encounter
- Power Consumption - PrimePower
  - 96.7 μW - $\Delta\Sigma$ modulator input is a tone at 1.6 kHz
  - 100 μW - $\Delta\Sigma$ modulator input is a white noise
- Active area = 0.46 mm^2

Layout of the fabricated chip



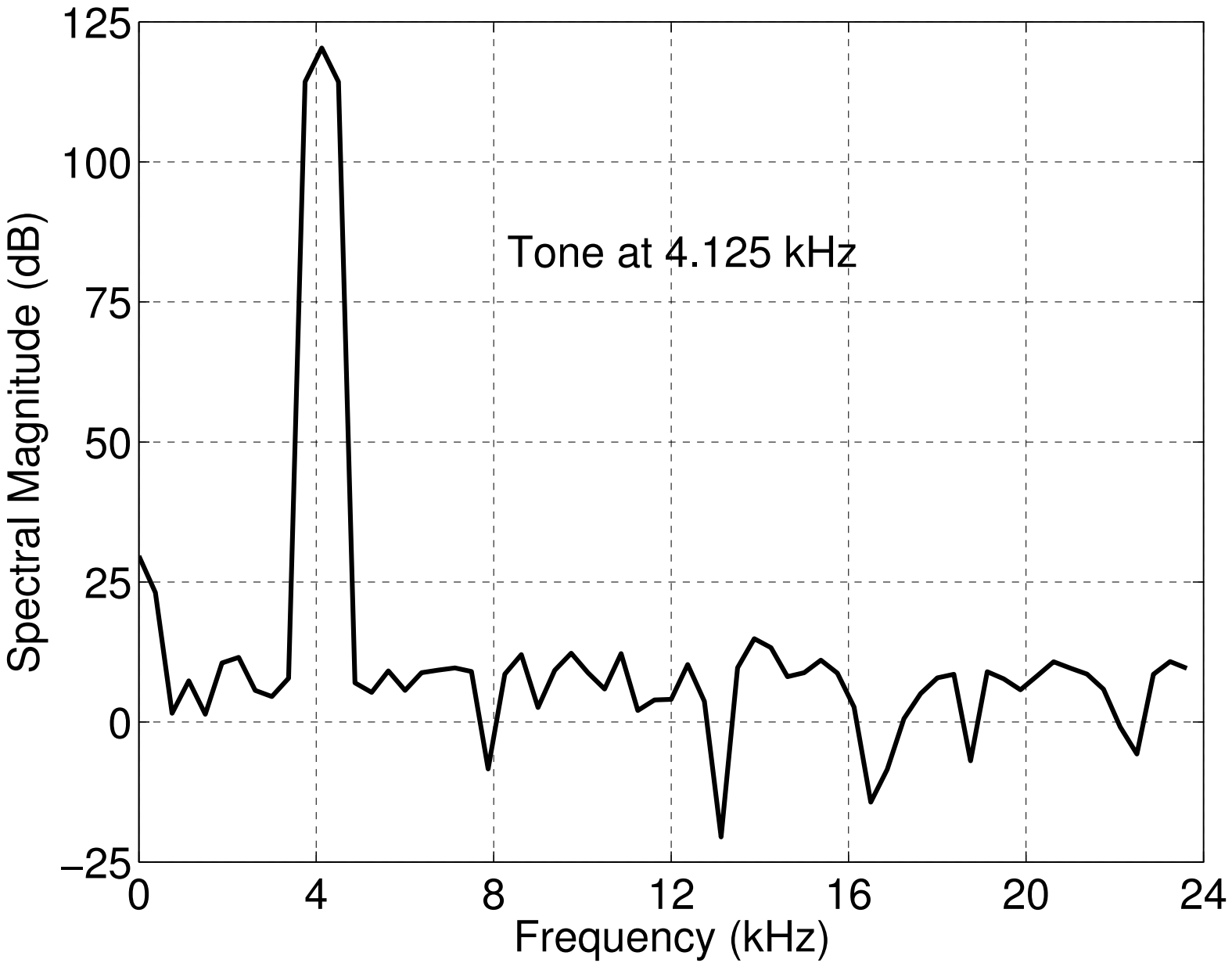
Picture of the test board



Measurement results from the chip

- Chip works correctly at 1.8 V supply and works reliably down to 0.9 V at 3.072 MHz
- Current consumed with 1.8 V supply = 58 μA (104.4 μW)
- Current consumed with 0.9 V supply = 26 μA

Decimated output spectrum from the chip



Conclusion

- 100 μW decimator for audio $\Delta\Sigma$ ADC
- No handcrafted circuits - completely implemented with automated CAD tools
- Works down to 0.9 V supply
- 50% power reduction with a linear power regulator

References

- S. Pavan, N. Krishnapura, R. Pandarinathan, and P. Sankar, "A power optimized continuous-time $\Delta\Sigma$ converter for audio applications," *IEEE Journal of Solid-State Circuits,* vol. 43, no. 2, pp. 351 360, 2008
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