EE685: VLSI Broadband Communication Circuits; HW3

Nagendra Krishnapura (nagendra@iitm.ac.in)

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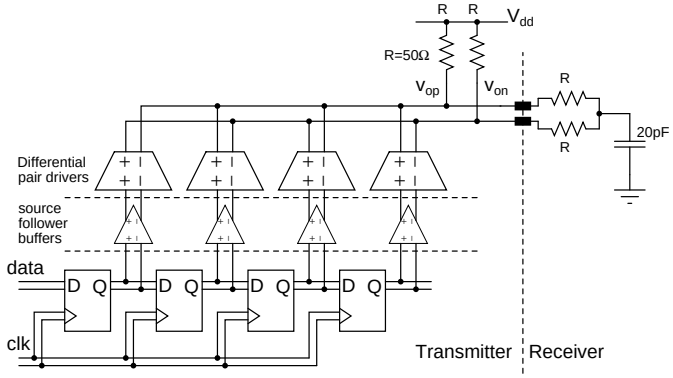

Figure 1: Transmit equalizer

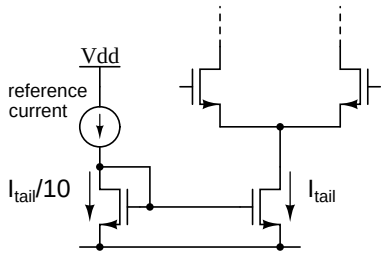

Figure 2:

1. Transmit equalizer: Design a 4 tap equalizer with the following normalized tap weights: $\{-0.25, 1.0, -0.5, 0.25\}$. Use the architecture in Fig. 1. The load side is represented by ac coupled resistors as shown in the figure. Do the design in the following steps, working backwards from the output. In each step, report, transistor sizes, bias values, and waveforms as appropriate.

1. Design (analytically) the differential pair driver stage for the largest possible output amplitude while maintaining all transistors in saturation by appropriately choosing the tail currents and input common mode voltage of the diff. pair driver. Fig. 2 shows the schematic of the differential pair realizing each coefficient. Use about 200 mV gate overdrive for the tail current source.

2. Carry out initial simulations with ideal delayed inputs with rise/fall time of 200 ps. Assume 600 mVppd differential input swing. The output rise/fall times (between 20% to 80% of the transition value) must be 200 ps. For doing this test, use an alternating bit pattern.

3. Add source follower buffering stages to drive the differential pairs. Design the source follower so that it can be driven from current mode logic stages and drive the differential pairs with the correct common mode voltages. Minimize the bias current the source followers while satisfying the output rise time requirements. Drive the source followers with ideal delayed inputs with rise/fall time of 200 ps with an appropriate amplitude and common mode voltage.

4. Drive the source followers with flip flops designed in the first assignment. You may have to increase the output amplitude of the flip flops and resize the flip flops so that they can drive the source followers. Also, you may have to com-

promise a bit on the output amplitude to get all the common mode levels correct.

5. Drive the channel in the previous assignment (for both 10% and 50% unequalized eye opening) with $v_{op} - v_{on}$. Show eye diagrams at the input and output of the channel. Do this with (a) Coefficients $= \{-0.25, 1.0, -0.5, 0.25\}$, (b) Coefficients determined in the previous assignment (least mean square). To adjust the coefficients, adjust the reference currents of differential pairs which realize tap coefficients (Fig. 2). Keep the cursor current at its maximum value.

2. PAM4 transmitter: Outline a scheme for a PAM4 transmitter. The input is a binary data stream at f_s bits/s and the output should be a PAM4 stream at $f_s/2$ symbols/s which can drive a differential transmission line terminated on either side by $50\,\Omega$ resistors (similar to Fig. 1).

Time taken to do the assignment: How many hours did you spend on this assignment? Of those, how many were spent in writing up the report?