

EE685: VLSI Broadband Communication Circuits; HW1

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0.18 μm technology parameters: $V_{Tn} = 0.5\text{ V}$; $V_{Tp} = 0.5\text{ V}$; $K_n = 300\text{ }\mu\text{A/V}^2$; $K_p = 75\text{ }\mu\text{A/V}^2$; $V_{dd} = 1.8\text{ V}$; $L_{min} = 0.18\text{ }\mu\text{m}$, $W_{min} = 0.24\text{ }\mu\text{m}$; $L_d = L_s = 0.36\text{ }\mu\text{m}$; Ignore body effect unless mentioned otherwise.

1. Design an nMOS current mode logic inverter which has an output peak-peak swing of 600mV differential and switches completely at 300mV peak-peak differential input.

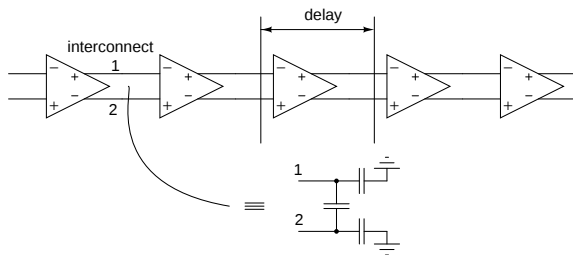


Figure 1: Problem 1

2. Simulate the chain of inverters as shown in Fig. 1. Model the parasitic capacitance of interconnects between inverters. Assume that they are on metal 2 layer, 10 μm long, 0.25 μm wide, and 0.5 μm apart. Scale the bias current to obtain 100 ps delay through each inverter. Delay is the difference between input and output zero crossings of the middle inverter.
3. Use the scaled inverter above to realize a latch. Keep the clock common mode to be 0.4 V below the data common mode. How would you

bias the clock at the correct voltage? You have a differential clock with zero common mode available to you (Hint: The clock is a high frequency periodic signal) Verify the latch with 1 Gb/s alternating data and 1 GHz clock.

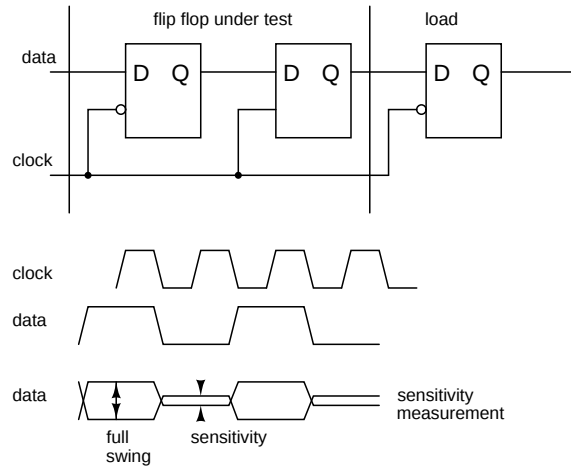


Figure 2: Problem 3

4. For this problem, use a clock with 50 ps rise/fall times. Use interconnect model from P1 on the data lines. Determine the sensitivity (with clock centered on the data), setup time, hold time, and clock to Q delay of a rising edge triggered flip flop (Fig. 2) for two cases: a) input alternating between $\pm$ sensitivity limit, b) input alternating between $\pm$ full swing. Assume that the latch/flip-flop is “working” if, at the end of the regeneration phase, the amplitude reaches 80% of the dc value. Timing of an event is defined by

the zero crossing of the corresponding differential waveform.

5. In a CML latch, suggest a way to change the time constant of sampling/regeneration relative to one another without changing the swing, bias current level, or transistor sizes. Justify.
6. (zero credit) How many hours did you spend on this assignment? Of those, how many were spent in writing up the report?

CML design procedure

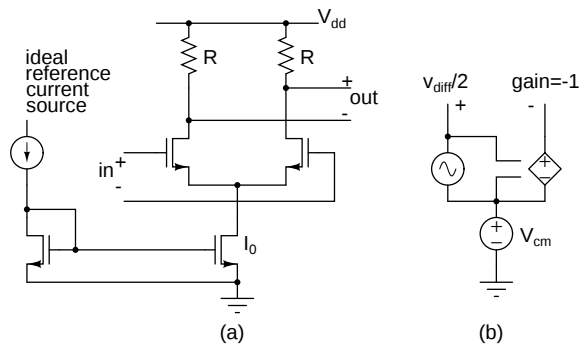


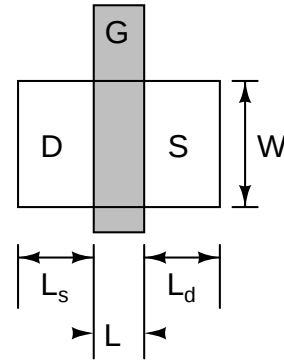
Figure 3: CML buffer

Fig. 3(a) shows a CML buffer. Briefly, the design procedure is as follows

- Use minimum length for the switching pair and longer devices for the bottom current source; Use a current mirror and *one* external current reference.
- From square law model and approximate process parameters, choose the sizes, I_0 , and R to satisfy the input and output swing requirements.
- Use simulations to confirm that the circuit works to specifications.
- Scale all currents and impedance levels up or down to satisfy the speed requirements without affecting the intrinsic characteristics of the gate.

Use the circuit in Fig. 3(b) to provide differential signals.

Source/drain parasitics of an MOS transistor



$$L_d = L_s = 0.36\mu$$

Figure 4: MOS layout

Add source/drain area and perimeter (as , ad , ps , pd) to your mos transistors. The layout of a transistor is given above. Drain and source diffusion regions have a length of $0.36\mu\text{m}$.