EE658: VLSI Data Conversion Circuits; HW5

Nagendra Krishnapura (nagendra@iitm.ac.in)

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Submit all solutions by email as a single pdf file; 0.18 μm technology parameters: $V_{Tn} = 0.5$ V; $V_{Tp} = 0.5$ V; $K_n = 300\ \mu\text{A}/V^2$; $K_p = 50\ \mu\text{A}/V^2$; $A_{VT} = 3.5\,mV\,\mu$m; $A_\beta = 1\%\,\mu$m; $V_{dd} = 1.8$ V; $L_{min} = 0.18\ \mu$m, $W_{min} = 0.24\ \mu$m;

1. Compute the signal and quantization noise transfer functions of the $\Delta\Sigma$ modulator in Fig. 1(a).

   Compute the signal to quantization noise rms ratio if the signal bandwidth is f_b and sampling rate is f_s.

   What is the sampling rate required for CD audio applications? (peak $S/N = 106$ dB, $f_b = 24$ kHz).

   What is the sampling rate required for CD audio applications? (peak $S/N = 106$ dB, $f_b = 24$ kHz) if the quantizer is oversampled without the use of noise shaping? (Fig. 1(b))

   What is the input sampling capacitor required if the signal to quantization and random noise combined is 100 dB? Assume that the sampled thermal noise is uniformly spread over the nyquist band.

2. In HW4, P3(h), it was assumed that the comparators consume 20 μA in all cases. This is not quite correct, as the comparator offset required, and hence its size and power dissipation, are dependent on the stage resolution. Compute the input transistor widths (use minimum lengths) for the comparator in each of the four architectures. Assume that

   - The comparator offset σ_{off} is $2\sigma_{VT}$ of the transistor.
   - The σ_{off} is required to be 0.1 LSB of that particular stage.

   If a comparator with minimum size transistors consumes 0.6 μA, compute the current consumption in each stage for all the architectures. Compute the total power consumption in the comparators and in the A/D converters. Compare them to the values calculated previously (assuming identical comparators)[1].

[1] While this problem accounts for different LSBs of the four architectures, it assumes no offset correction, which changes the game further

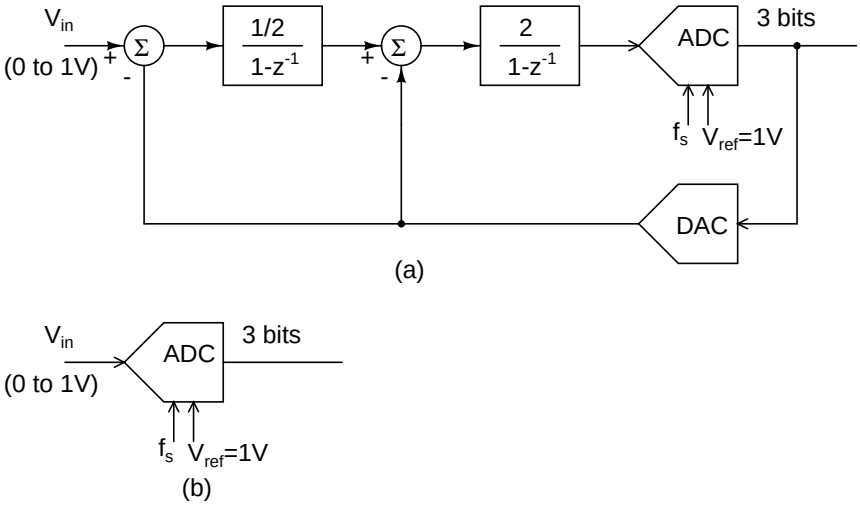
V_in
(0 to 1V)
+
-
Σ
1/2
1-z^-1
+
-
Σ
2
1-z^-1
ADC
3 bits
f_s
V_ref=1V
DAC
(a)
V_in
(0 to 1V)
ADC
3 bits
f_s
V_ref=1V
(b)

Figure 1: