EE658: VLSI Data Conversion Circuits; HW3

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due on 17 Oct. 2005

Submit all solutions by email as a single pdf file; 0.18 μm technology parameters: $V_{Tn} = 0.5$ V; $V_{Tp} = 0.5$ V; $K_n = 300\ \mu\text{A}/V^2$; $K_p = 50\ \mu\text{A}/V^2$; $A_{VT} = 3.5\,mV\,\mu$m; $A_\beta = 1\%\,\mu$m; $V_{dd} = 1.8$ V; $L_{min} = 0.18\ \mu$m, $W_{min} = 0.24\ \mu$m;

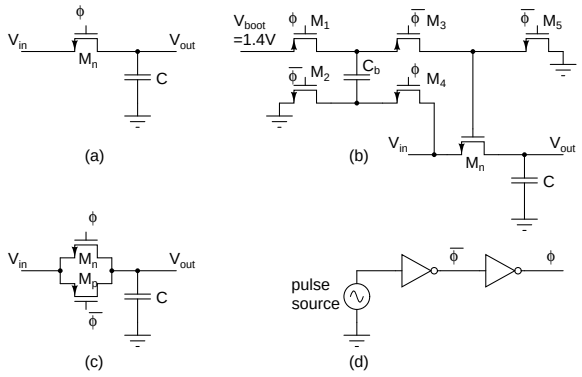

Figure 1:

1. Sample and hold circuits: Fig. 1 shows 3 sample and hold circuits. $V_{in} = V_{cm} + v_{in}$. $V_{cm} = 0.4V$ for nMOS S/H, $V_{cm} = 0.9V$ for complementary S/H, $V_p = 0.3\,V$ max.

   What is the hold capacitor value C to have an output thermal noise 70 dB below the signal rms?

   Simulate the circuits in track mode. Determine the switch size for a small signal tracking bandwidth of 1 GHz. For the complementary switch, size the nMOS and pMOS transistors for equal contributions to bandwidth.

   Use the circuit in Fig. 1(d) to drive the circuit in Fig. 1(a) at a sampling rate of 1 GHz. Determine the inverter size for a rise/fall time of 50ps(10% to 90%) at the gate of M_n. Assume that the input pulse source has 100 ps rise/fall times.

   Where would you connect the bulk node of the pMOS transistors in Fig. 1(b)?

   Simulate Fig. 1(b) and determine the sizes of M_{1-5} such that the waveform at the gate of M_n has a rise/fall time of 50 ps. Use $C_b = 0.25C$. For this simulation, use ideal pulse sources for ϕ and $\bar{\phi}$ with 50 ps rise/fall times. Then drive Fig. 1(b) with Fig. 1(d) and resize the inverters for 100 ps rise/fall times(10% to 90%) at the gates of M_{1-5}.C

   Simulate each of the three S/H circuits designed above with f_s = 1 GHz, $v_{in} = V_p \cos(\omega_{in} t)$, $V_p = 0.15$ V and $V_p = 0.3$ V at input frequencies of $1/64 f_s$ and $33/64 f_s$. In each case report the strength of the fundamental, the second, and the third harmonic (use a 64 point DFT). Plot the waveforms at the input, output, and the gates of $M_{p,n}$. Comment on the results.

   Simulate each of the three S/H circuits designed above with f_s = 1 GHz and dc inputs of $v_{in} = \pm 0.15\,V$ and $v_{in} = \pm 0.3\,V$. Determine the track to hold pedestal in each case.

2. Latch circuits: Simulate the latch in Fig. 2. Use minimum size nMOS transistors in the latch.

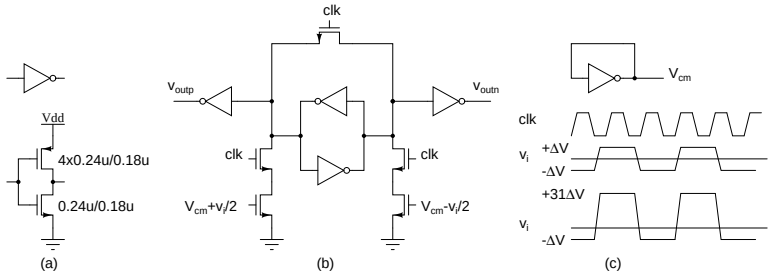

Figure 2:

Generate the input common mode voltage using a self biased inverter as shown. What is V_{cm}?

Simulate the circuit with $T_{clk} = 1\,\text{ns}$, 100 ps rise/fall times, and an alternating input-simulate 2 cases: alternating between $\pm\Delta V$ and alternating between $+31\Delta V$ and $-\Delta V$. Run the simulation for ΔV from 5 mV to 15 mV in steps of 1 mV. Find out the lowest ΔV that still results in correct latch decisions. This is the sensitivity of the latch.

Compute 3σ of the V_T mismatch between the input transistors.

Plot the current consumption of the latch for one cycle and compute the average power dissipation.

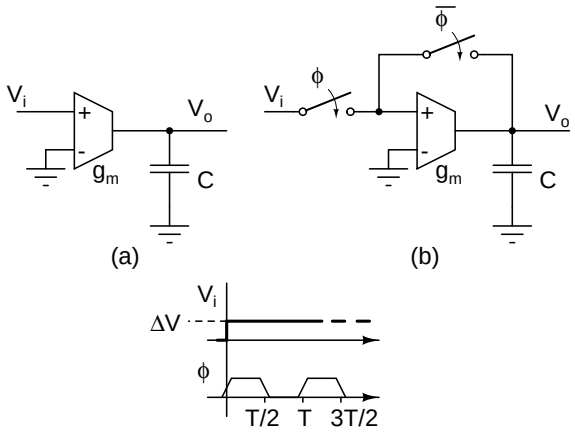

Figure 3:

3. Amplifier vs. positive feedback latch: Assuming zero initial conditions on the capacitors, calculate the output voltage of the circuits at the end of the time period T in Fig. 3 for a step input. What is the dynamic gain (ratio of the output at the end of the time period T to the input step) of each circuit? Which one would you prefer to use in a comparator? Do the calculations for for $C/g_m = T/4$ and $C/g_m = T/8$.

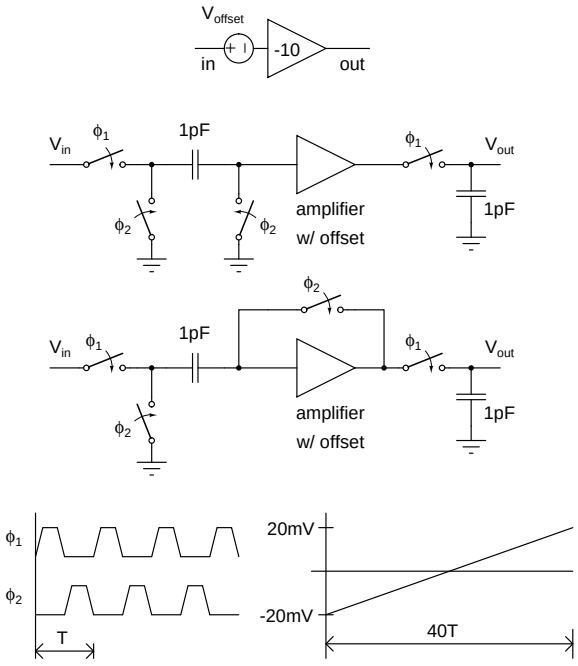

Figure 4:

4. Simulate the two configurations shown in Fig. 4 for amplifier offsets of 0 V and 10 mV. Plot the outputs(overlaid). Explain the results.