EE658: VLSI Data Conversion Circuits; HW2

Nagendra Krishnapura (nagendra@iitm.ac.in)

due on 15 Sep. 2005

Submit all solutions by email as a single pdf file; 0.35 μm technology parameters: $V_{Tn} = 0.6$ V; $V_{Tp} = 0.7$ V; $K_n = 150\ \mu\text{A}/V^2$; $K_p = 40\ \mu\text{A}/V^2$; $A_{VT} = 5\,mV\ \mu$m; $A_\beta = 1.5\%\ \mu$m;

1. Compute the effect of the output impedance on the single ended and differential DACs in Fig. 1. Is there a difference? What is the G_o/G_l ratio that can be tolerated for 1/2LSB maximum error in a 10 bit DAC in the two cases? G_o is the output conductance of a cell when it is on.

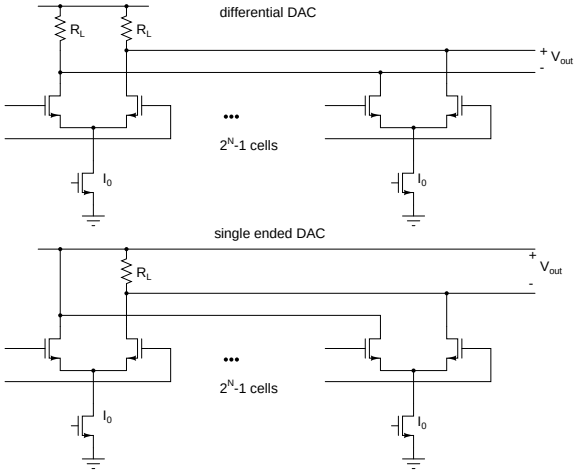

Figure 1:

2. An 8 bit thermometer coded DAC is realized as shown in Fig. 2(a). Relate the standard deviation of the DNL to the standard deviation σ_{I0} of the relative error in each current source δ_{Ik}/I_0. Find σ_{I0} such that the standard deviation of DNL is 0.1 LSB.

   Simulate the INL and DNL of this DAC by creating 255 current sources with appropriate *random* δ_{Ik}/I_0. Repeat the simulations 32 times with independent random δ_{Ik}/I_0 each time. This is equivalent to measuring INL and DNL of 32 nominally identical DACs with random errors. Calculate the standard deviation of INL and DNL at each input code (i.e. standard deviation $\sigma_{INL}[n]$ of $INL[n]$) over the 32 DACs. Is the computed value of $\sigma_{DNL}[n]$ consistent with the calculations in the previous part? What is $\max(\sigma_{INL}[n])/\sigma_{I0}$? How many times would you have to increase the size of the current source array in order to have $\max(\sigma_{INL}[n]) = 0.5$ LSB?

   An 8 bit binary weighted DAC is realized as shown in Fig. 2(b). It consists of 255 current sources. Input bit b_k controls 2^k current sources. The standard deviation σ_{I0} of the relative error in each current source δ_{Ik}/I_0 is the same as in the thermometer coded DAC in the previous problem. How does the INL of this DAC compare to the INL of the thermometer coded DAC? How about the DNL? Calculate the standard deviation of the DNL at the following code transitions: a) 01111111 to 10000000, and b) 00111111 to 01000000

3. A 8 bit thermometer coded DAC has a linear gradient in the current sources. The rela-

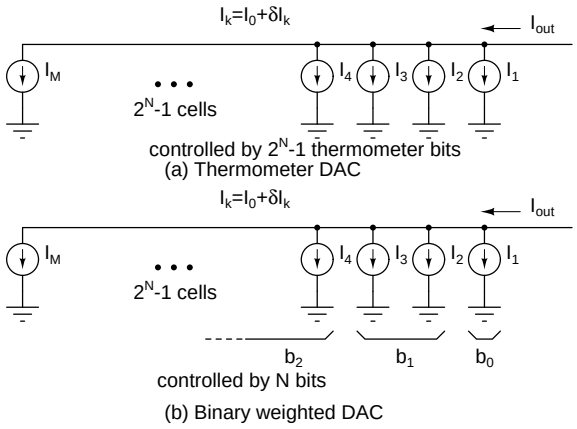

Figure 2:

tive increment between two successive current sources is 2^{-10}. Plot INL and DNL in the following cases: a) sequential switching, b) symmetrical switching, c) Random shuffling of the current sources(try 16 random permutations-plot all curves on the same plot). Report maximum INL and DNL in each case.

4. A 8 bit DAC is built using the current steering cells shown in Fig. 3.

   The full scale(differential) output voltage of the DAC needs to be 2.04 V. Calculate the lower limit on the switch voltages V_{bi}, V'_{bi}.

   The switching voltage $V_{bi} - V'_{bi}$ has a peak to peak value of 1 V. Calculate W and L for M_1 and M_2 for complete switching at 0.8 Vpp (to provide for some margin).

   Calculate the minimum and maximum voltages on the tail node n_1.

   Assuming a $V_{GS} - V_T$ of 0.8 V for the tail current source, calculate its dimensions such that the standard deviation in DNL is 0.01 LSB.

   Calculate the minimum supply voltage for proper operation of this circuit.

5. Simulate the circuit designed in the previous

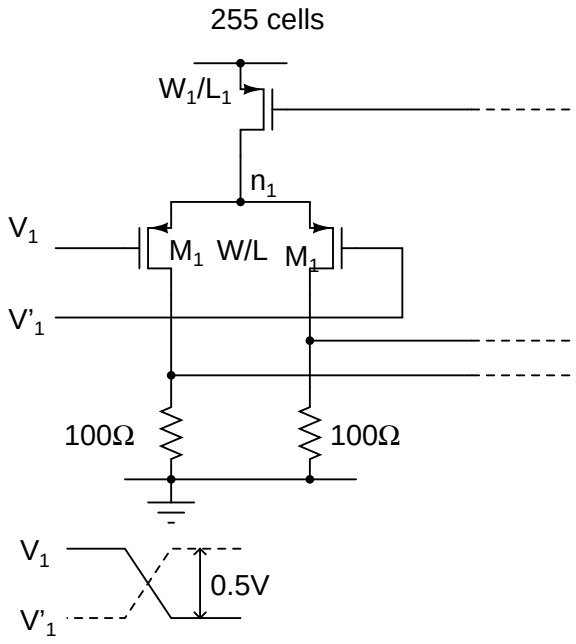

Figure 3:

problem with a power supply of 3 V. Use the values of swiching voltages V_{bi}, V'_{bi} calculated earlier. Simulate the configuration shown in Fig. 4(a)[1]

Simulate the full scale output of the DAC.

Simulate the output voltage waveform when the DAC inputs change from all zeros to all ones. Find the time required to settle to 0.25LSB. This is the sampling period.

Simulate the output voltage waveform when the DAC inputs change from all zeros to all ones and switch back to all zeros after a sampling period. Also simulate the case where the unit cell control voltage changes from zero to one and back to zero after a sampling period. Multiply the latter waveform by 255 and overlay it

[1] In Fig. 4(a), the DAC is divided as a parallel combination of a unit cell and a cell that is 254 times the unit cell. Setting up 255 unit cells and simulating them with thermometer coded inputs takes a long time. Combining the cells as shown reduces the time required to setup and run the simulations

on the full scale waveform. Is the larger waveform(full scale pulse) a scaled version of the smaller waveform(lsb pulse)?

Plot the waveform on the tail node as the control switches from zero to one. For the control waveforms, use a rise time that is 10% of the sampling period calculated in the previous part. Redo the simulations when the waveforms cross at the top and the bottom (Fig. 4(b)).

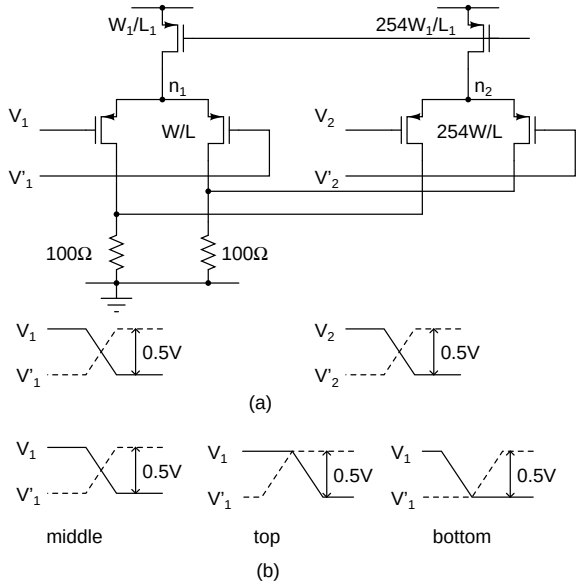

Figure 4: