EE658: VLSI Data Conversion Circuits; HW1

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(Only P2 needs a handwritten solution. Submit the rest by email)

1. Simulate one cycle of a sinewave passing through the quantizer. Divide the quantizer step into 50 steps and plot the histogram(with a total of 10000 points) of the quantization error. How does the simulated distribution compare to the uniform distribution that is commonly assumed? Do the simulations using a sinewave that spans the full quantizer range for 3, 7, and 11 bit quantizers (mid riser type).

   Plot the spectrum of a sampled quantized sinewave(using a 256 point DFT-and log-y axis). The input frequency of the sinewave must be near $f_s/4$. Compute rms quantization error and compare it to the theoretical value. Is the spectral density of quantization error constant over the frequency band? How large is the largest tone relative to the signal? Are there frequencies missing from the output spectrum? Why?

   Plot the spectrum of the quantized signal before sampling[1] and compare it to the one after sampling.

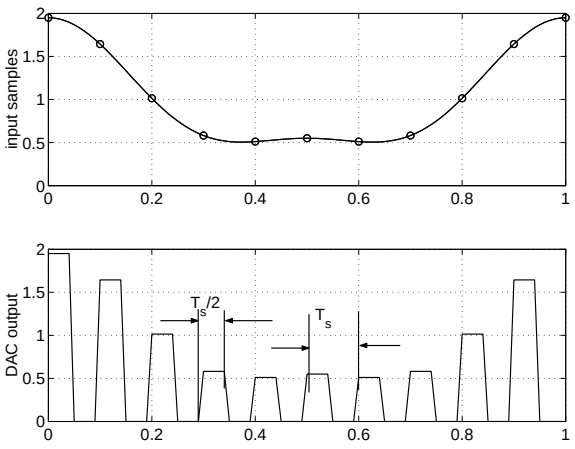

Figure 1: DAC with half width output pulses

2. DAC jitter: A DAC is designed to give half width rectangular output pulses. Compute the output spectrum of the DAC in terms of the spectrum of the digital input sequence $D_{in}[n]$. Compare this to the spectrum of a DAC with full width output pulses.

[1] This is a continuous-time signal. You need to approximate this by using a much higher sampling rate.

Compute the effect of jitter on the output of this DAC. How is it different from that in a DAC with full width output pulses?

3. DAC nonlinearity: Plot the INL and DNL of the 2 DACs whose output voltages are given in `dac1.txt` and `dac2.txt`. Note the maximum INL nad DNL. Simulate the output spectrum of the DAC with a full scale (digital) sinewave input near 1/4 the sampling frequency. Plot the input spectrum and the output spectrum of the 2 DACs. Compute SFDR, SNDR, and SNR for each case[2]. What can you say about the first DAC?

4. A/D nonlinearity: The output code density of an A/D converter to a low frequency full scale sine wave is given in `a2dcodes.txt`. How many bits does the A/D converter have? Analyze the code density to obtain its INL and DNL. Simulate this A/D converter with a full scale sinewave near half the sampling rate. Compute SFDR, SNDR, and SNR. What is the ENOB of this converter? What is the maximum jitter that can be tolerated so that the SNR due to jitter is 3dB more than the SNDR computed above?

[2]Ignore dc for all these cases. Assume that everything other than the largest spurious tone is noise.