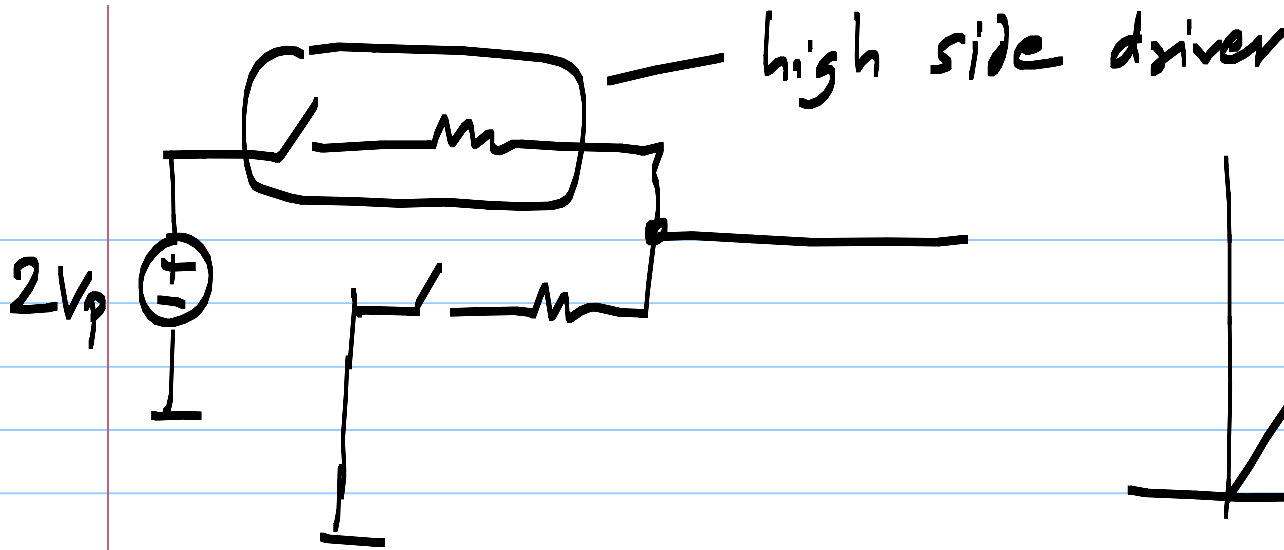
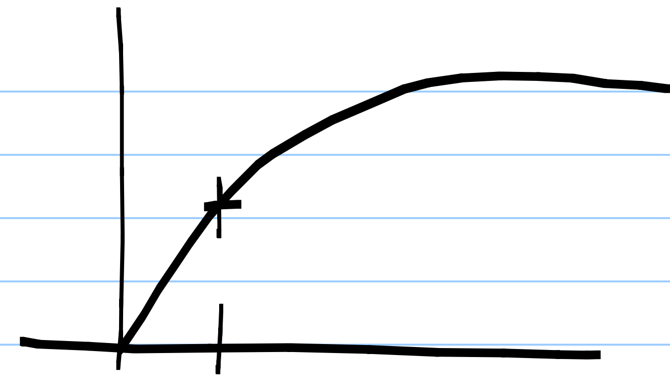
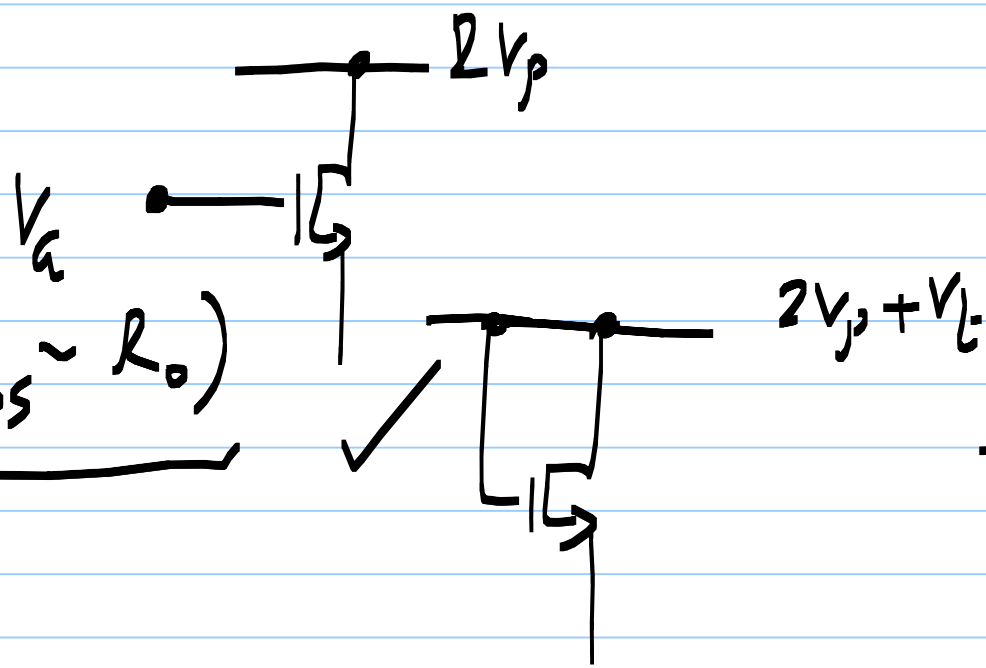
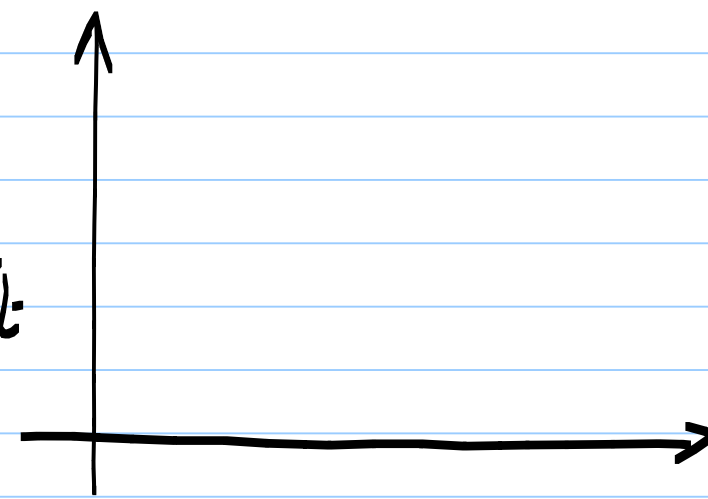


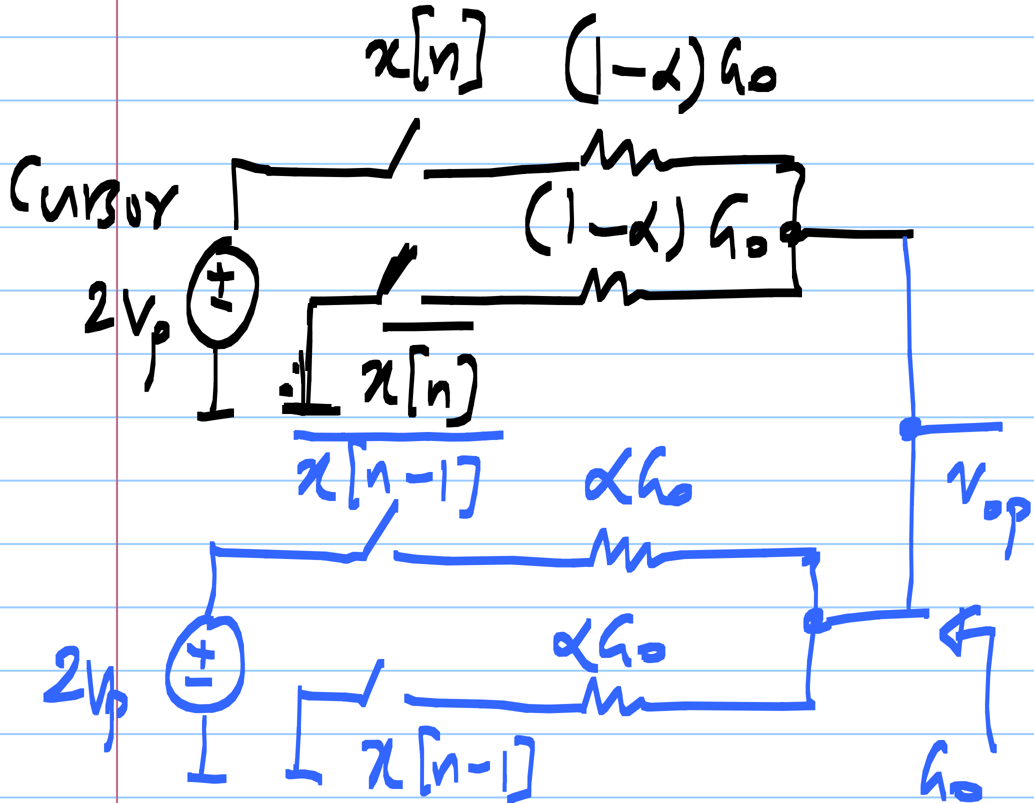



$(R_{mos} \sim R_o)$



# Differential implementation of the voltage mode transmitter with equalization

$(1-\alpha)\,x[n] - \alpha\,x[n-1]$

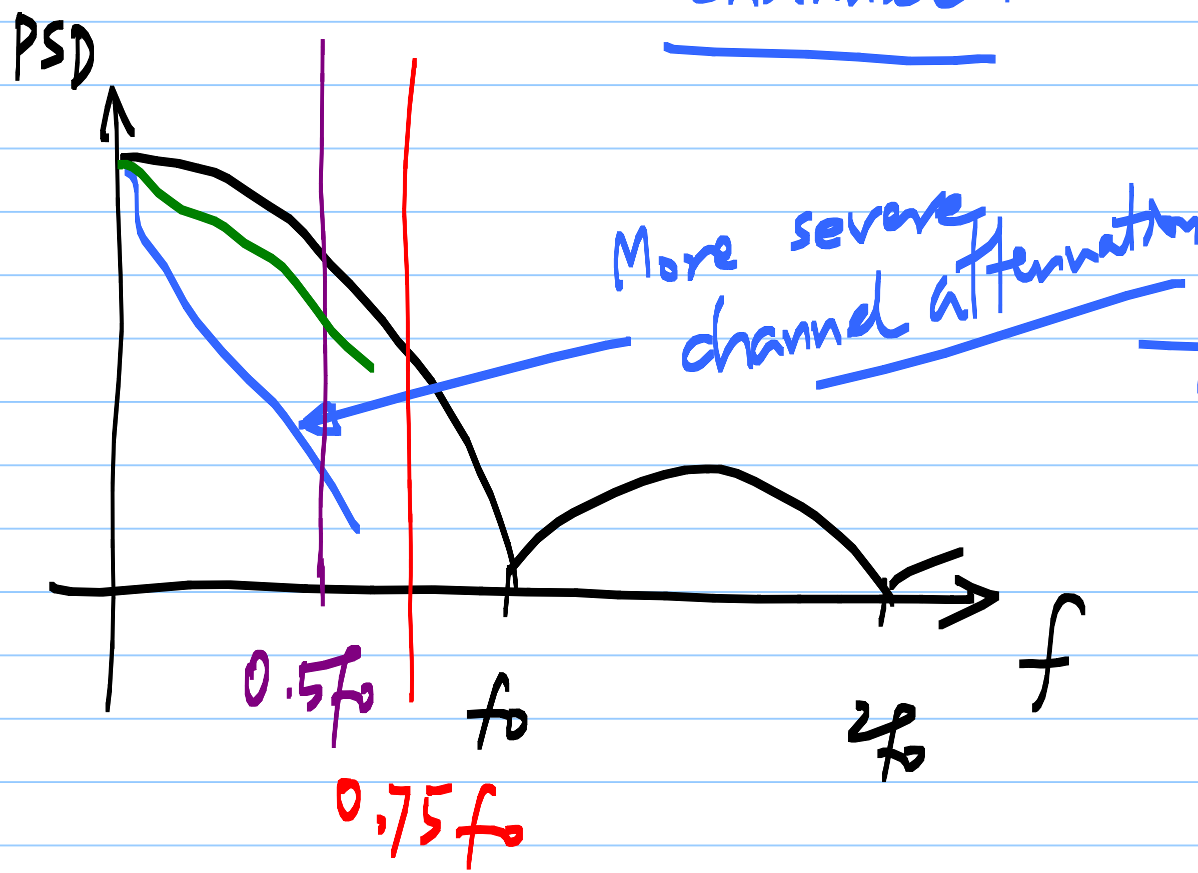


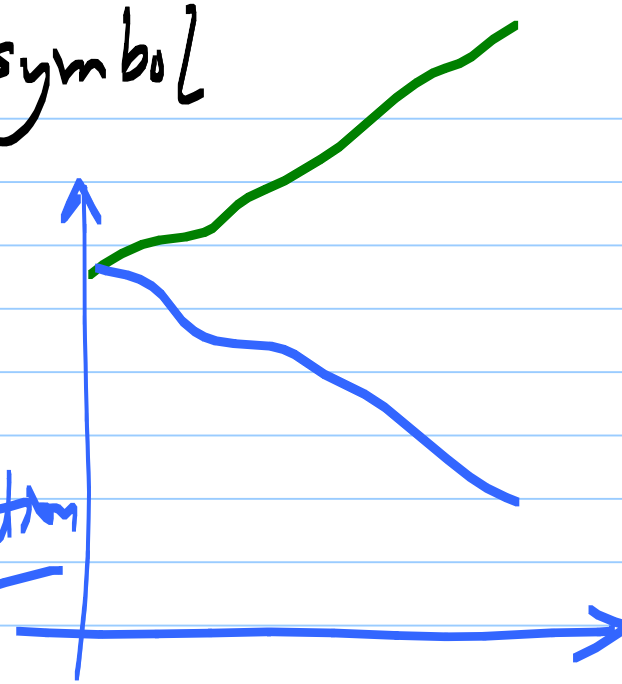
## Binary transmission : 1 bit/symbol

$\pm 1$

@ $f_0$ b/s

channel:



$f_0$ has been increasing

Data rate: ~ 10s Gb/s

56, 112 Gb/s

Binary: 28GHz, 56GHz

Very difficult to realize circuits of 56GHz bw

Signaling schemes with reduced bandwidth: Increase # b/symbol

# Transmit more than 2 levels in a symbol period

PAM4 : Pulse amplitude modulation - 4 levels

2 bits / symbol interval

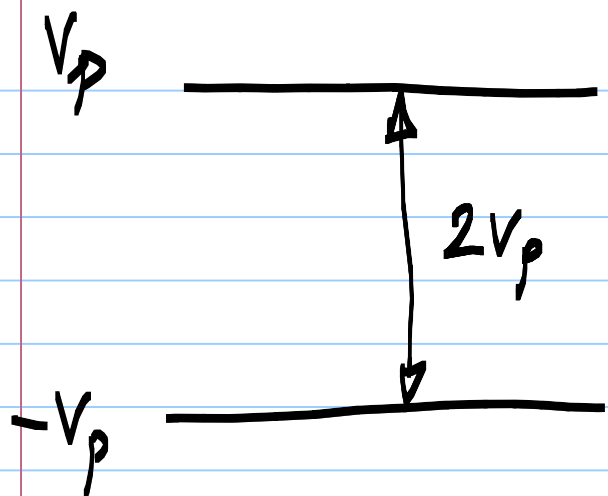
Binary @ 112 Gb/s [Nyq. freq = 56 GHz]

PAM4 @ 56 GS/s = 112 Gb/s

(2b/symbol) [Nyq. freq = 28 GHz]

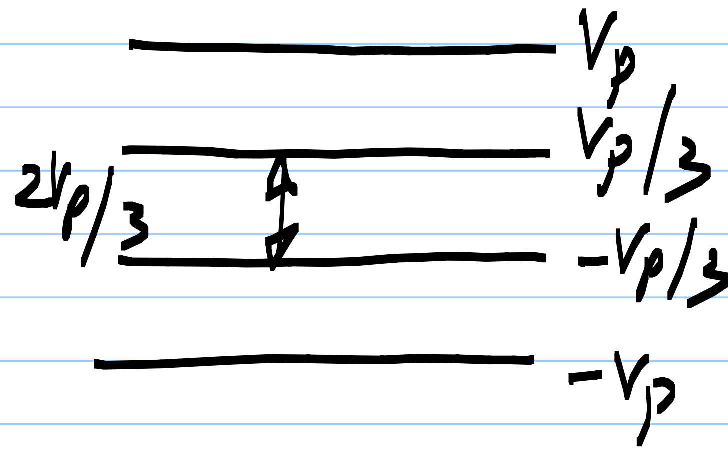
56 Gbaud

2 levels




Binary

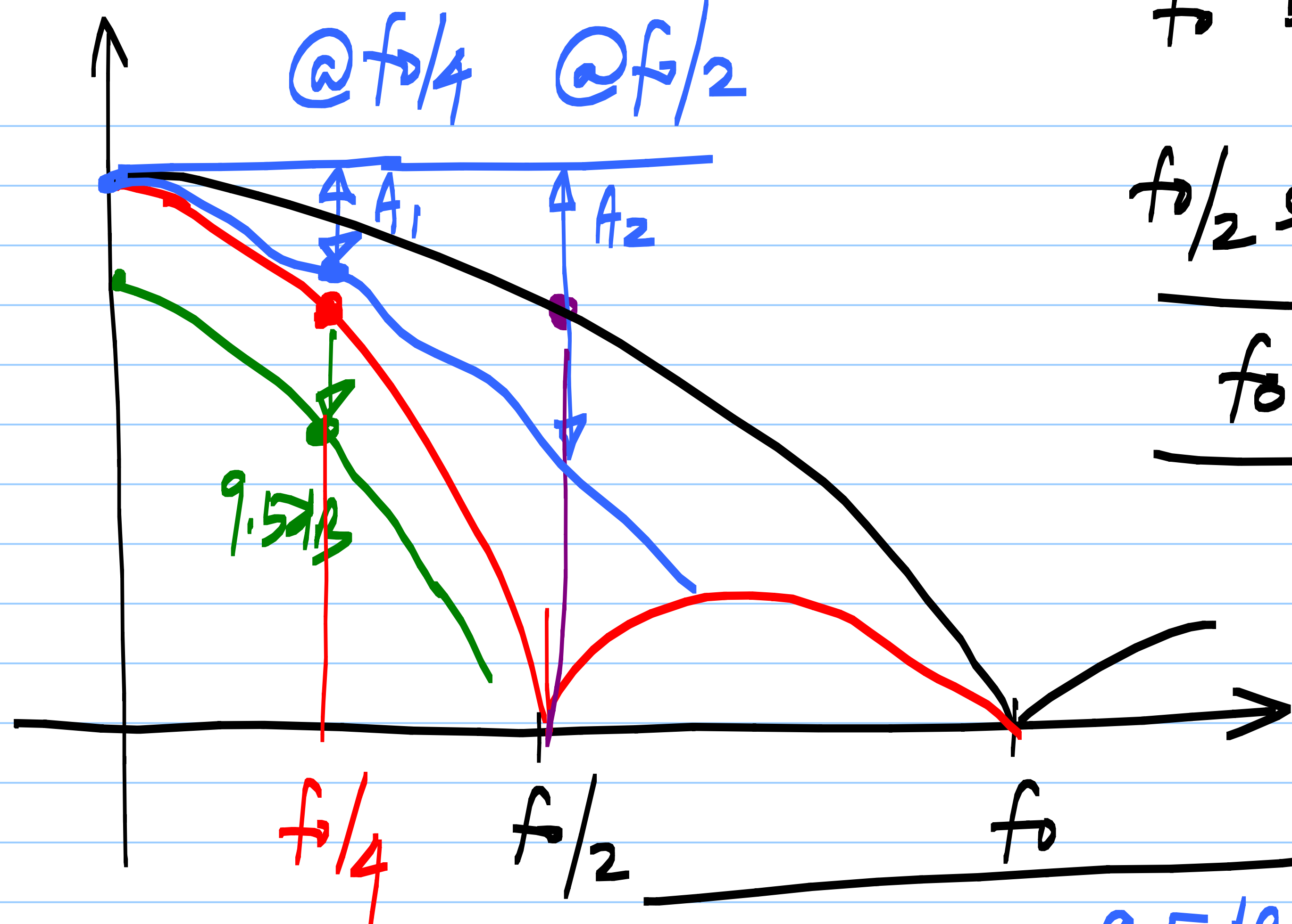
4 levels




PAM4

Level separation $= \frac{1}{3}$ (−9.5dB)

SNR lower by 9.5 dB




f0 b/s (Rectangular)

f0/2 s/s (PAM4)

f0 b/s

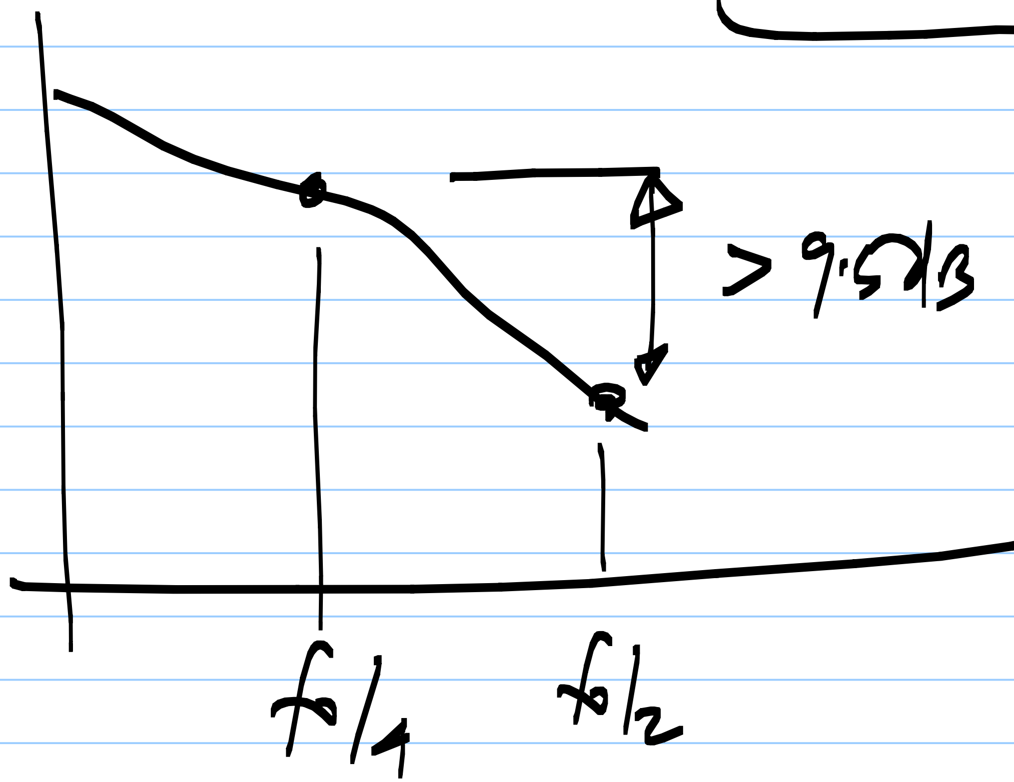
$A_1 - A_2 > 9.5\,dB$ ; PAM4 wins

$p(t)$

$$\sum \underbrace{x[n]}_{\text{white}} p(t - nT_s) \longrightarrow |P(f)|^2$$

Alternating bit pattern: $-V_p, V_p$ @ $f_0$

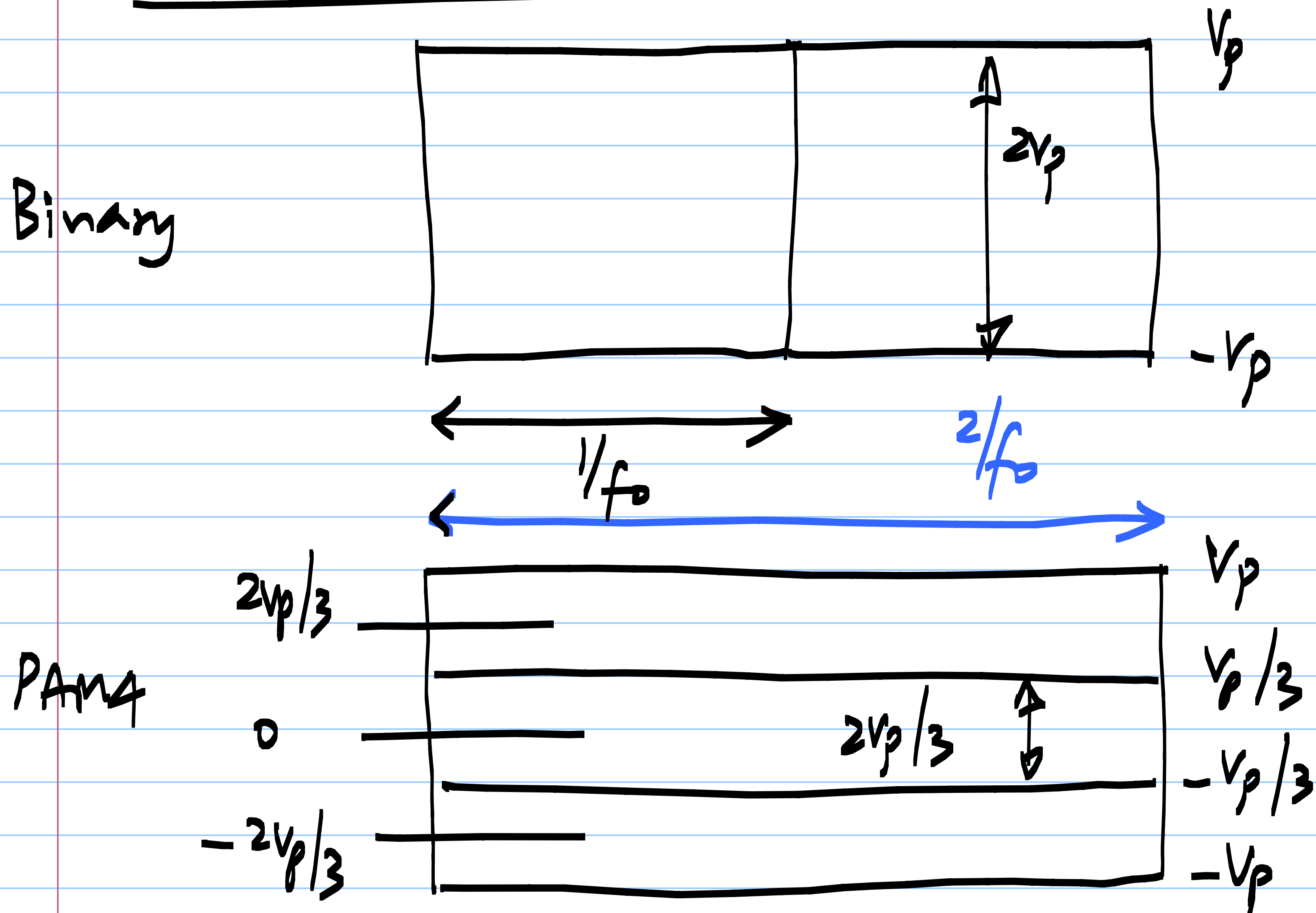
(PAM4) $-V_p/3, V_p/3$ @ $f_0/2$



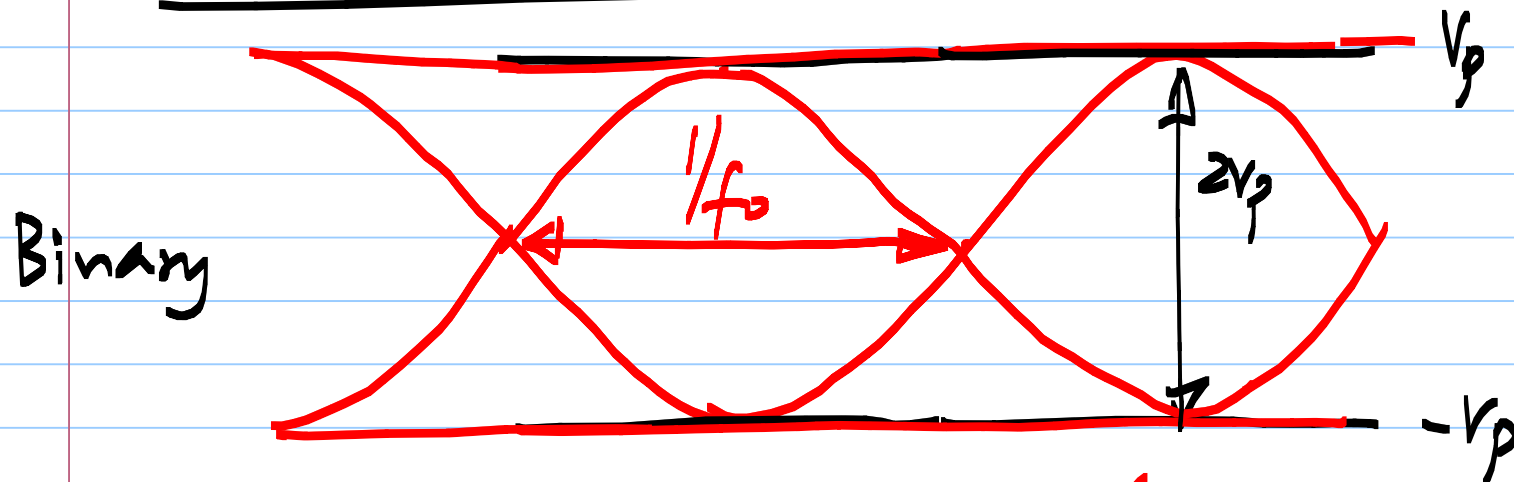
Transmission @ $f_0$ b/s

PAM4 is advantageous if attenuation @ $f_0/4$ is much less than attenuation @ $f_0/2$

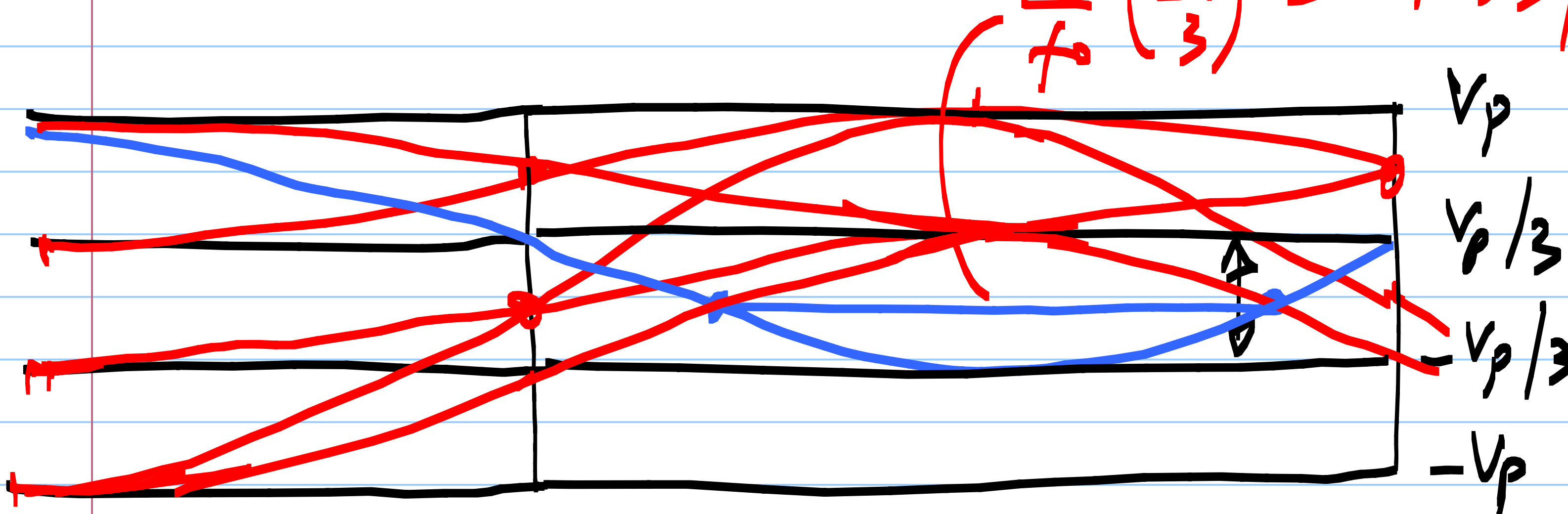
# Eye: Rectangular and PAM4

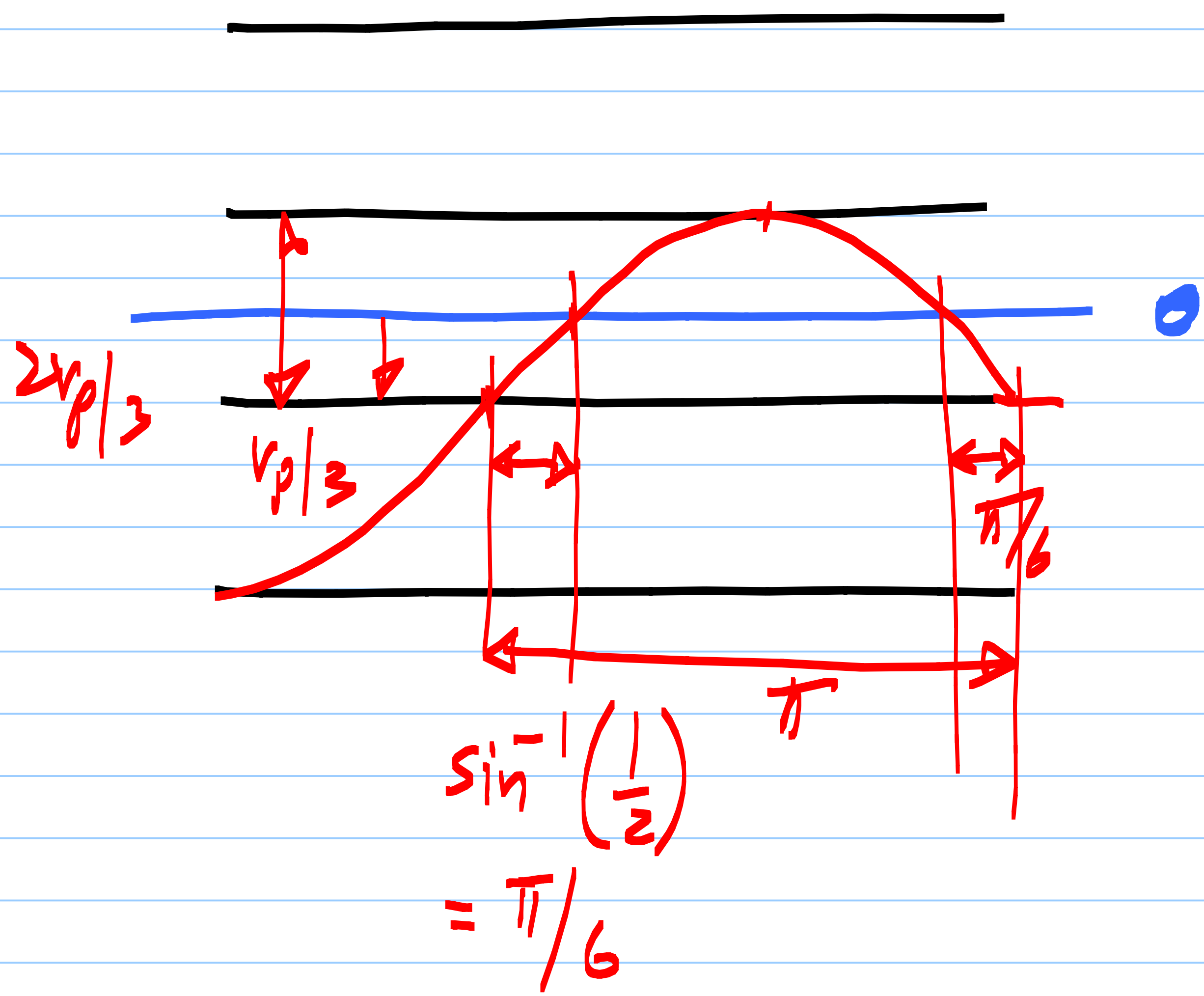


# Eye: Rectangular and PAM4




$\frac{2}{f_0}\left(\frac{2}{3}\right) = 1.33/f_0$

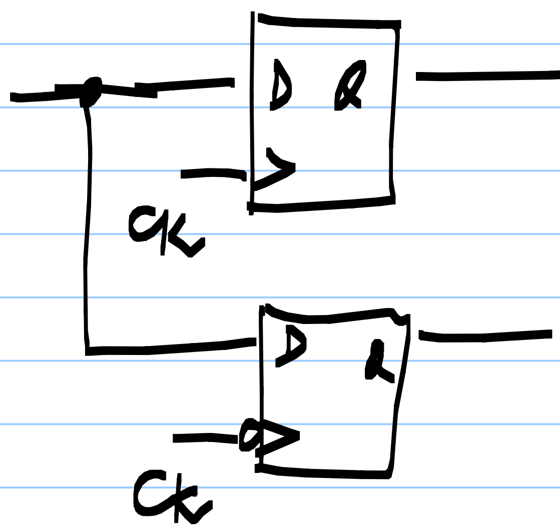




θ
2Vp/3
Vp/3
π/6
π
sin⁻¹(1/2)
= π/6

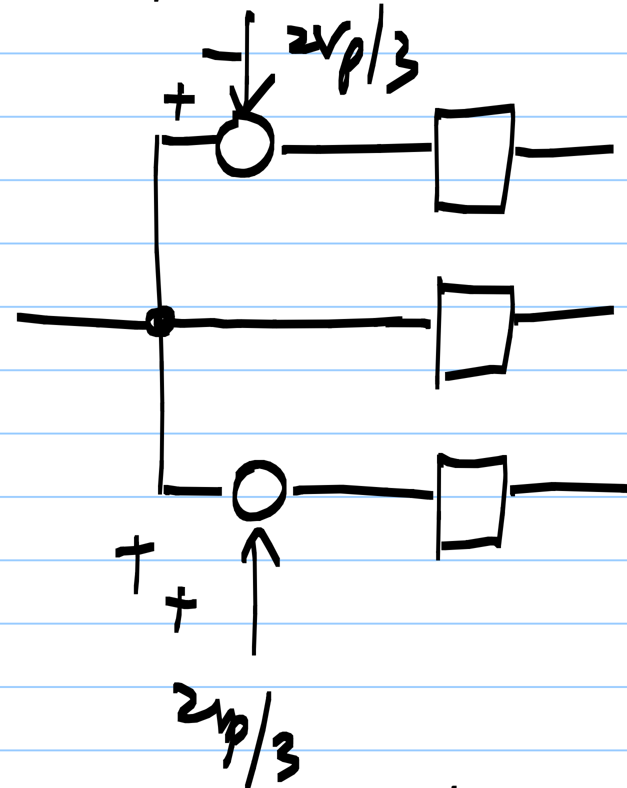
# Complexity:

Binary $R_x$




1 decision latch
1 transition

PAM4 $R_x$




3 latches
(decision

PAM4: ($f_0$ b/s) vs Binary ($f_0$ b/s)

- 50% signal bandwidth
- 1/3 peak voltage between adj levels (Fixed peak value)
- 33% more horizontal eye opening
- Tx, Rx more complex
  - Decisions, CDR, DFE, Tx, FFE (CTLE: same complexity)

PAM4 used at very high speeds (56/112Gb/s) links