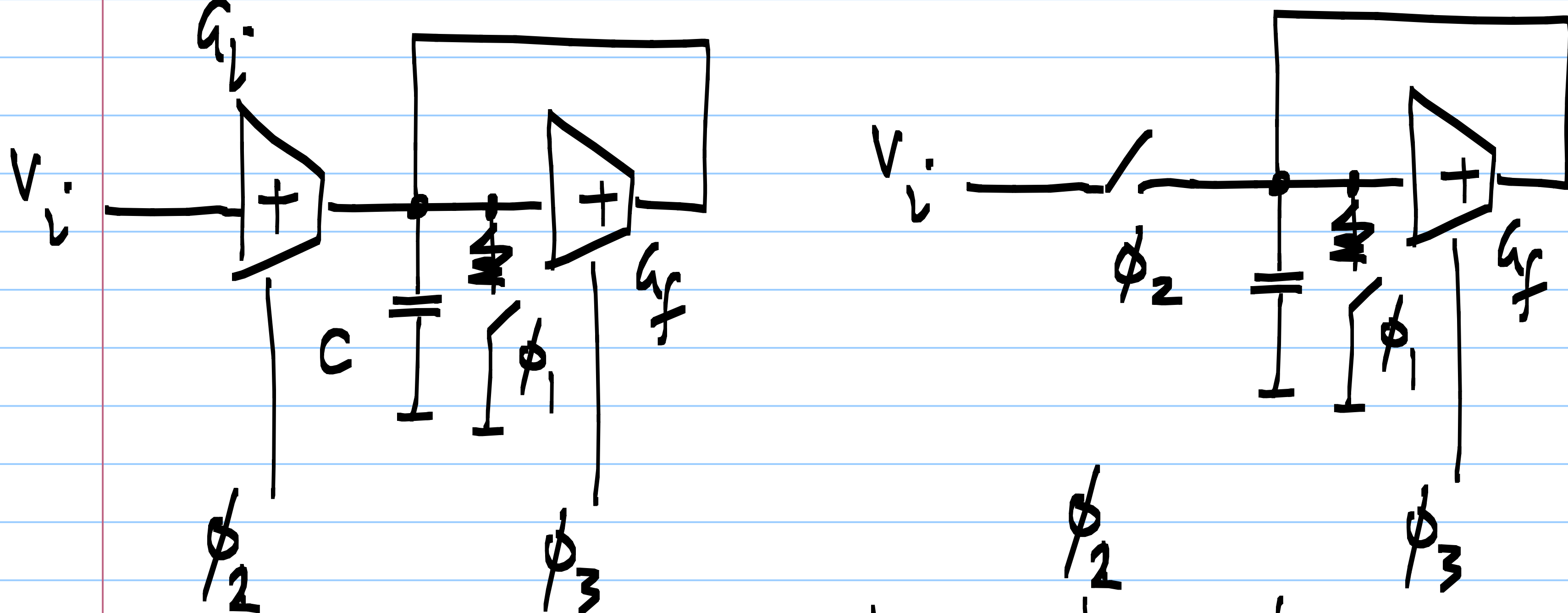
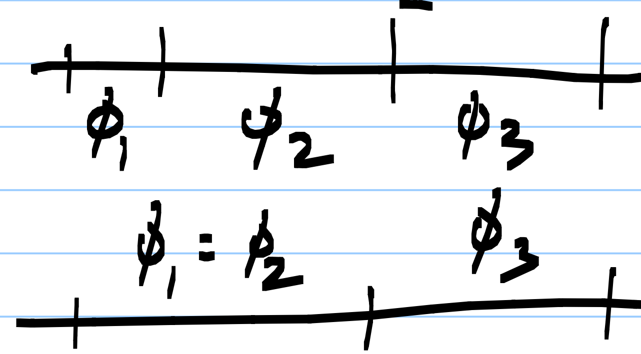
Latch implementation

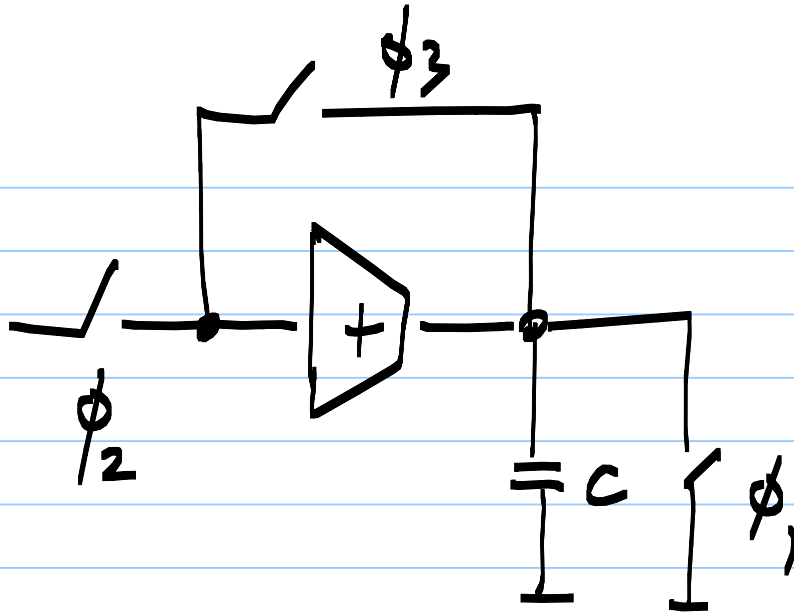


ϕ_1 : reset

ϕ_2 : sample

ϕ_3 : regeneration





ϕ_3
ϕ_2
+
C
ϕ_1

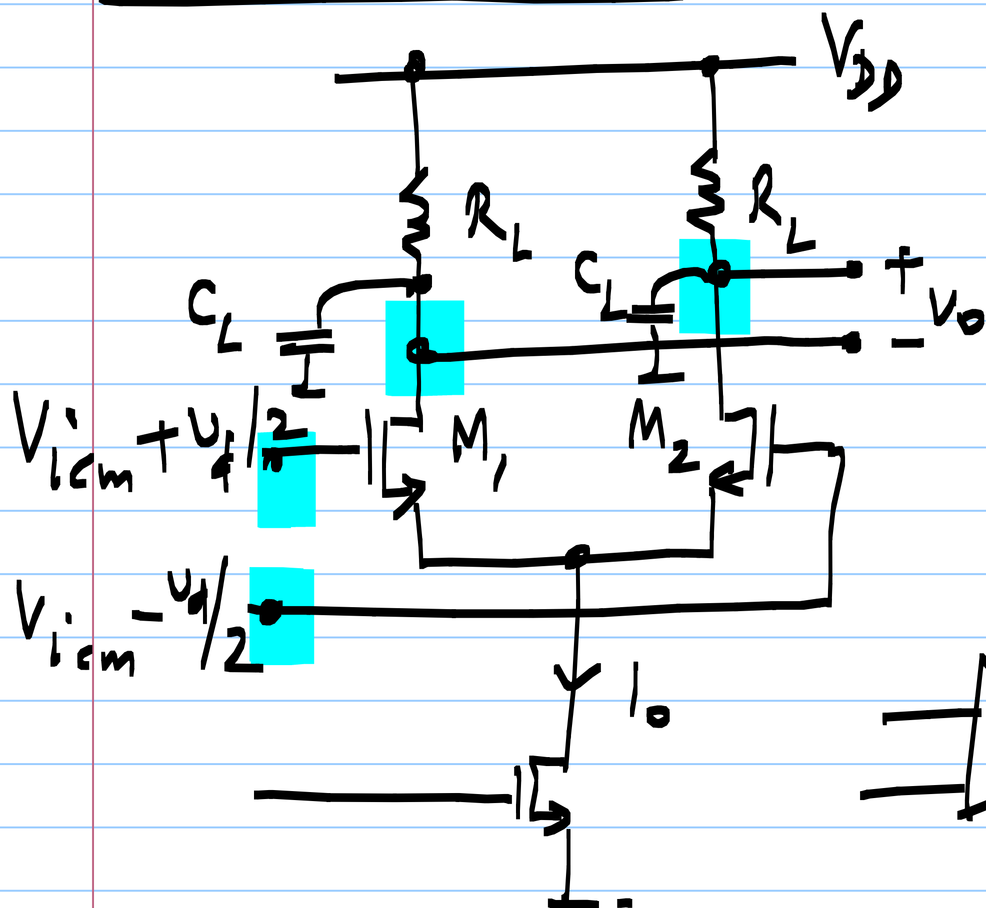
- Latch implementation

Fully differential / pseudo-differential

- Receiver circuits — CDR - Latches
  - Equalizer (CTLE)
  - VGA
  - DFE taps
  - Deserializer (demultiplexer) - Latches

- Tx circuits — Tx driver
  - Equalizer taps
  - Serializer (latches)

Rx amplifiers:

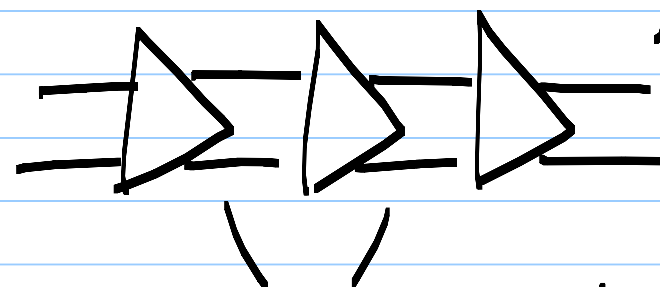


Variable gain:

* Vary R_L, I_o
* switched diff. pairs

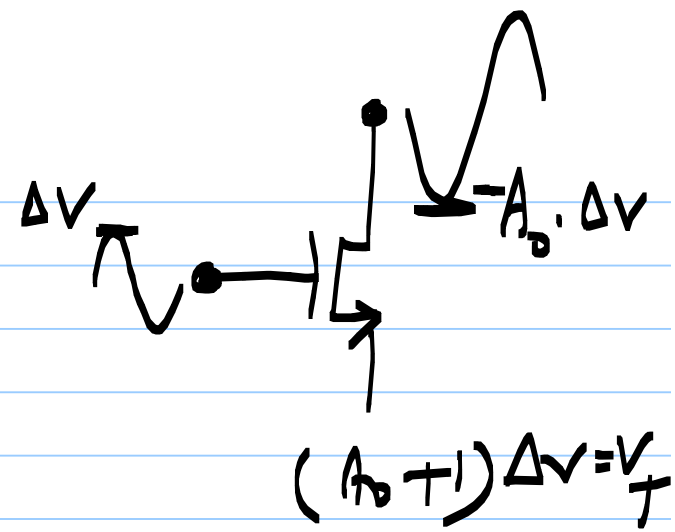
$$\text{gain} = \frac{v_o}{v_d} = g_m R_L;$$

$$BW = \frac{1}{R_L C_L}$$



$$V_{icm} = V_{ocm} = V_{DD} - I_o R_L / 2$$

Multiple stages in cascade

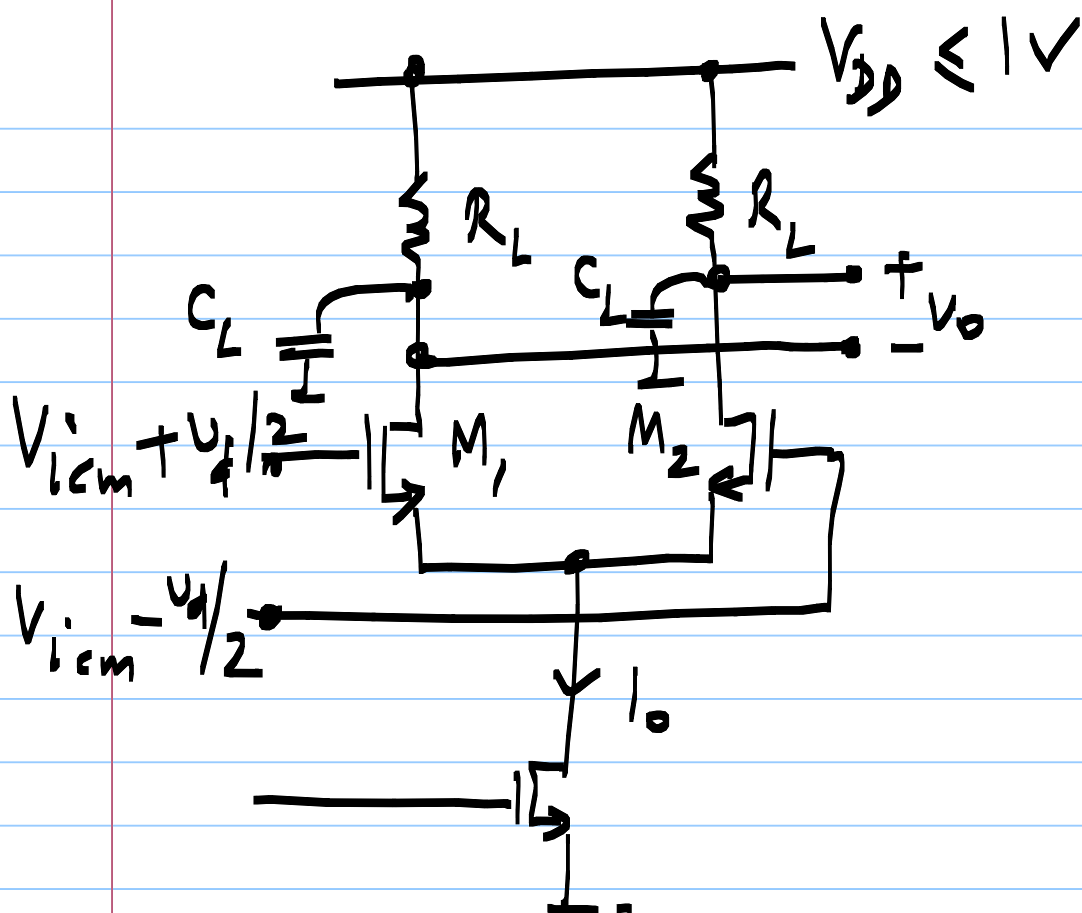


* $V_{ocm} \doteq V_{icm}$
* Peak swing at each input $= V_T/(A_0+1)$

Close to L_{min} for the transistors

$\Rightarrow g_{ds}$ can be significant

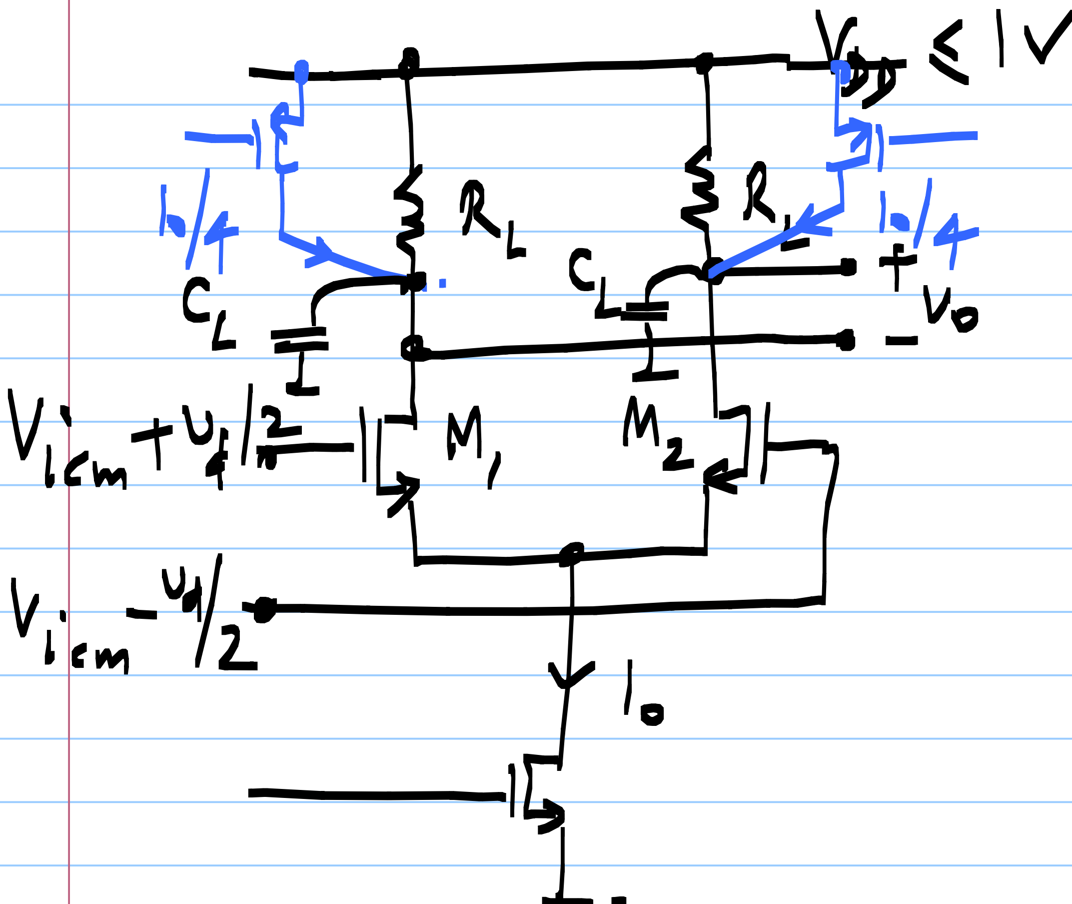
$g_m \cdot (R_L \| r_{ds})$



Higher gain:

Reduces $V_{O,cm}$;

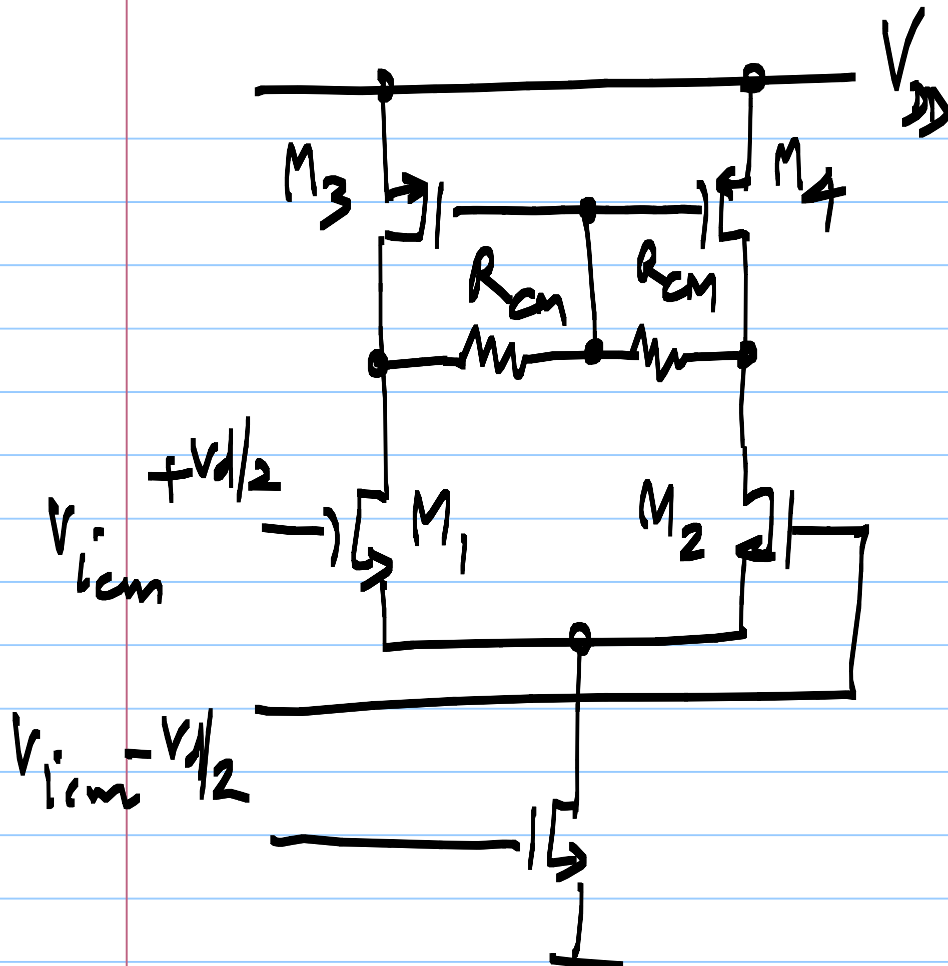
Cannot accommodate all transistors



$$V_{ocm} = V_{DD} - \frac{I_0}{4} \cdot R_L$$

2x R_L for same V_{ocm}

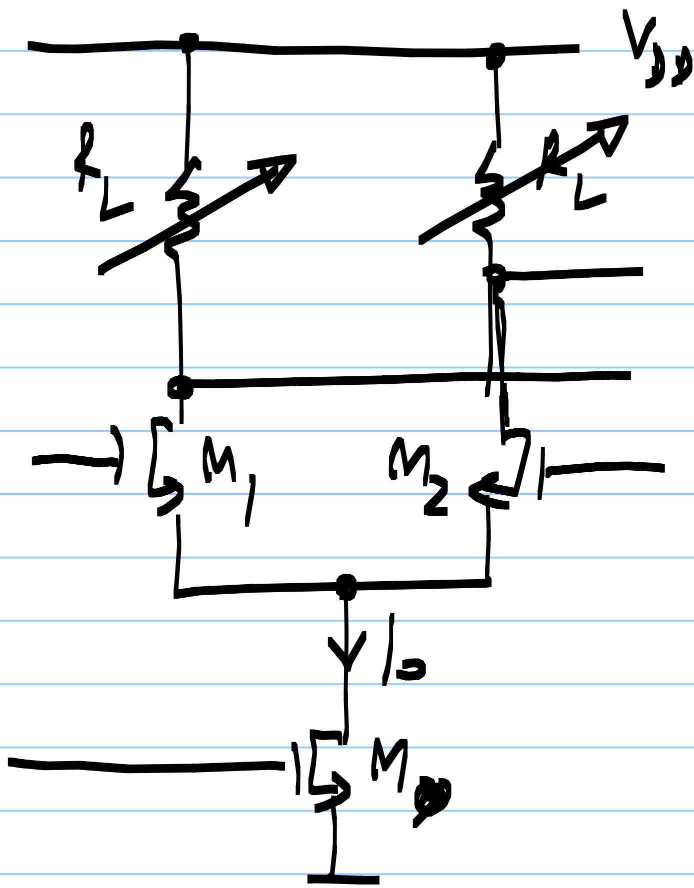
Additional parasitic due to the pMOS transistor ⇒ BW↓



High dc gain ;

Low BW

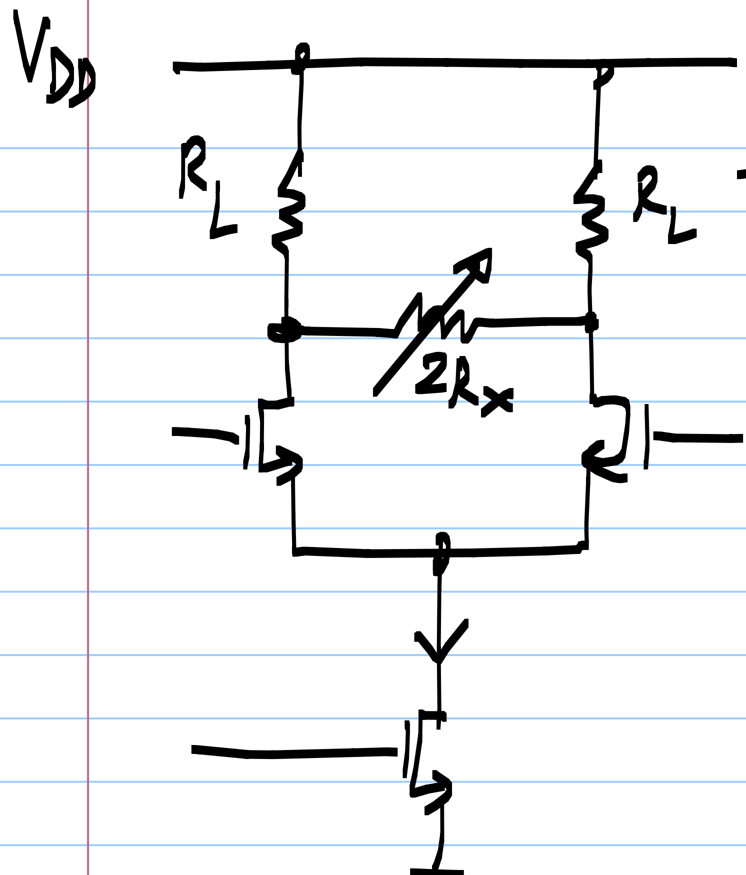
Variable gain by varying R_L, I_0



V_{ocm} changes with gain

Vary I_0:

* gain, V_{ocm} change
* linear range of the diff pair changes



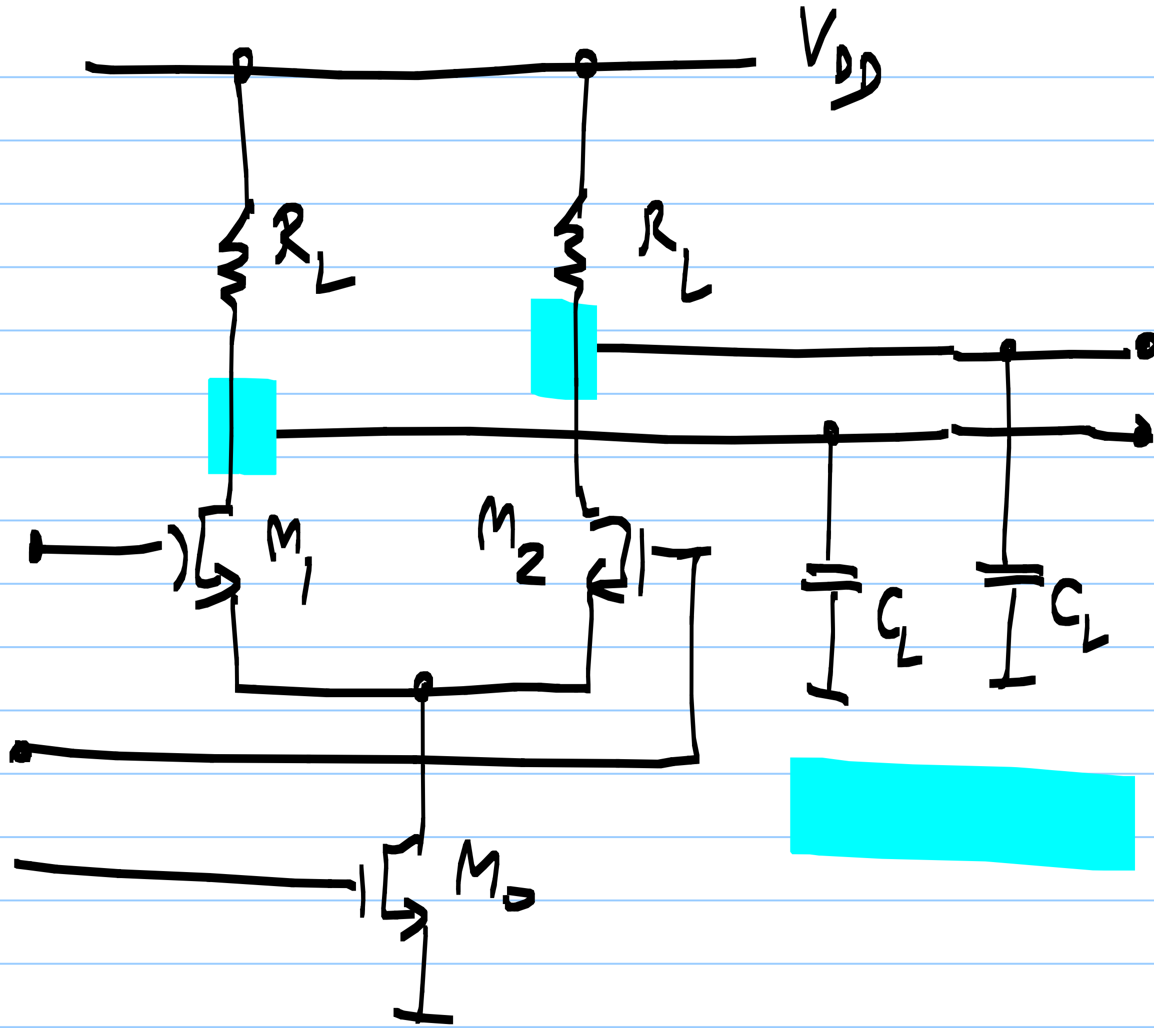
For max. gain

$g_m \cdot (R_L \| R_x)$

$V_{ocm} = V_{DD} - I_o R_L/2$

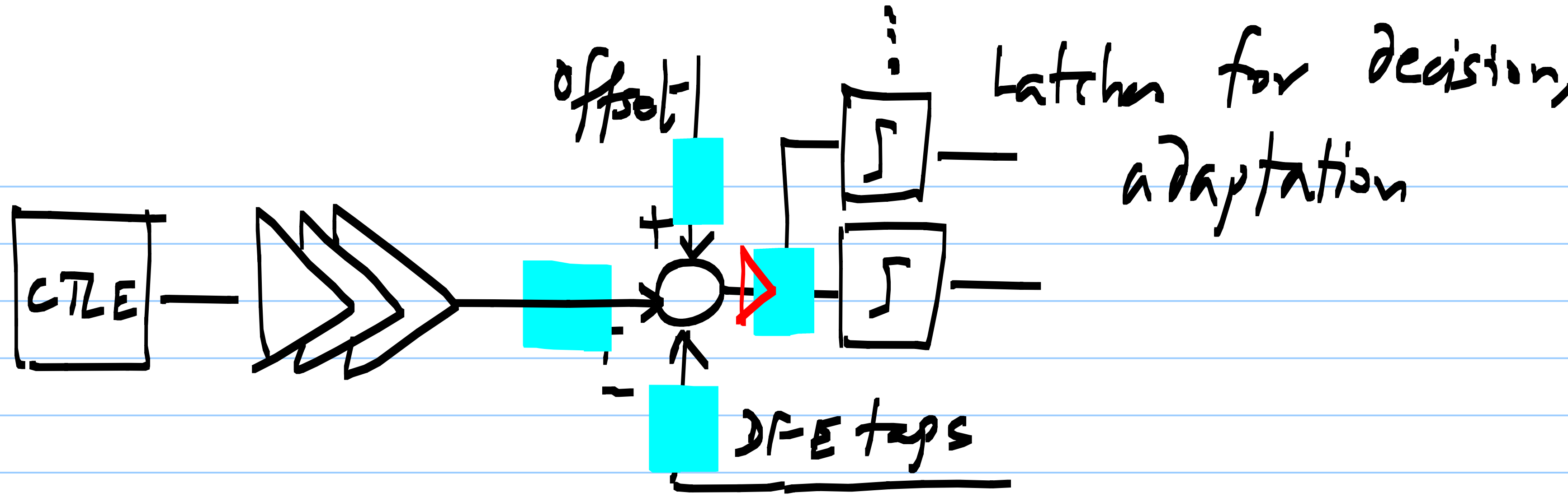
Can also be used with active load

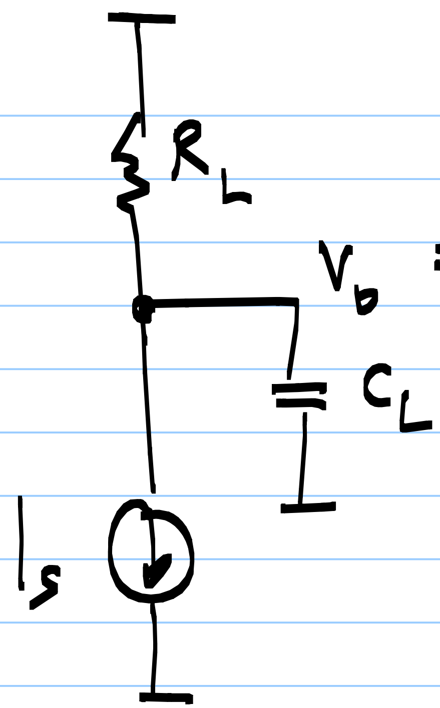
* Switch I_o, R_L, Diff pair
  - Change in V_{ocm} } Fix these
  - change in BW }



$$BW = \frac{1}{R_L C_L}$$

How to increase BW?

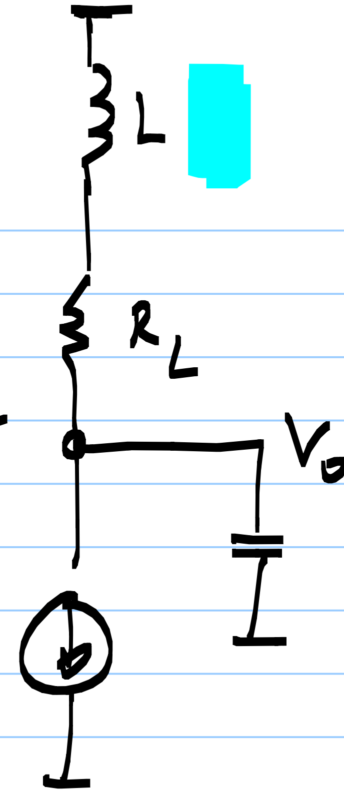

CTLE
offset
+
-
DFE taps
Latches for decision, adaptation



(diff. pair)

$$V_o = \frac{I_s \cdot R_L}{1 + sC_L R_L}$$

low Q factor



Series inductor peaking.

choose L for broad-band-response

Inductors – large area

→ Active inductor