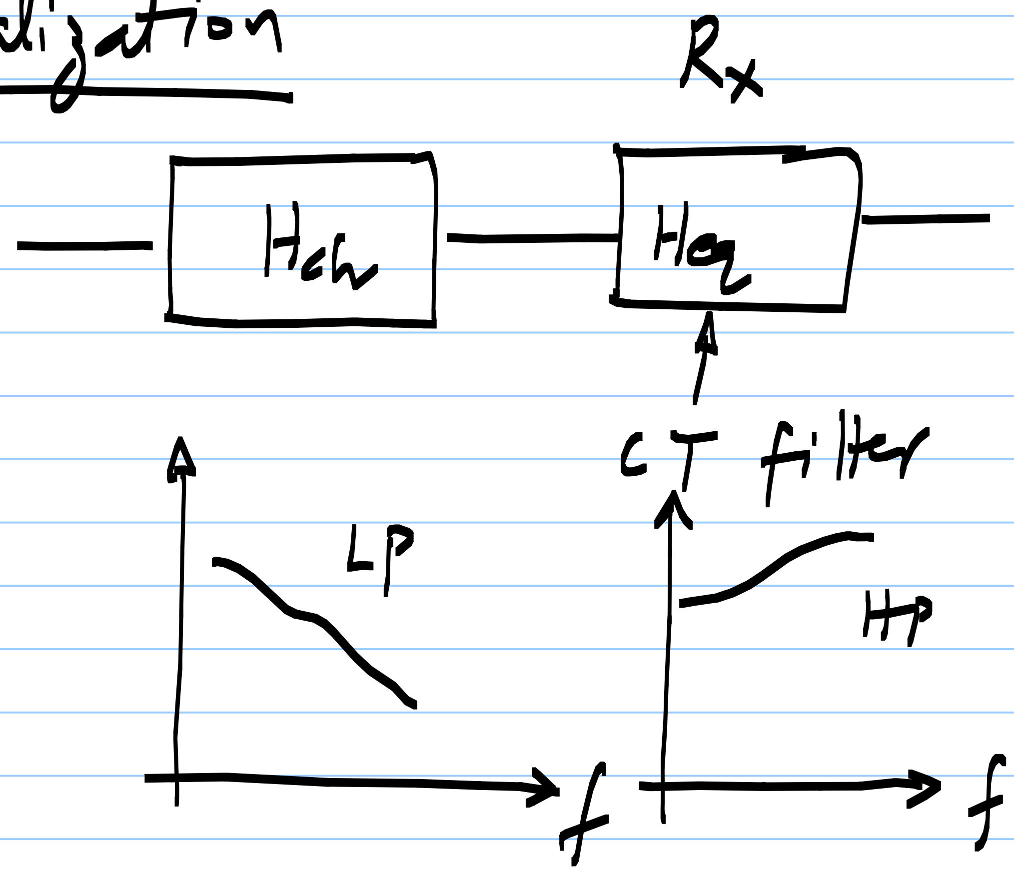
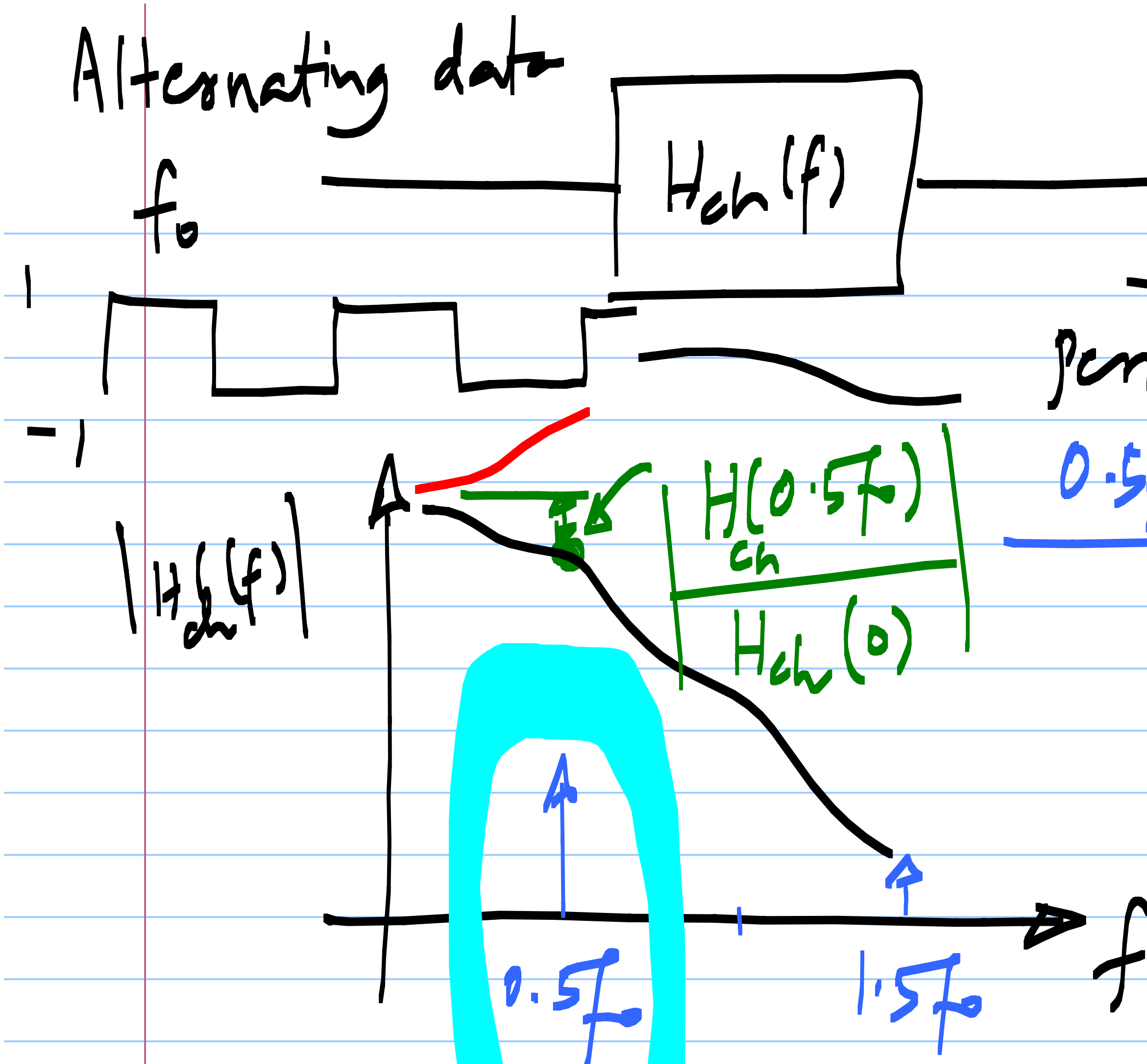
Equalization: Reduce ISI

CT equalization



$$\frac{1 + \text{[illegible]}}{(1 + s/p_1)(1 + s/p_2)}$$



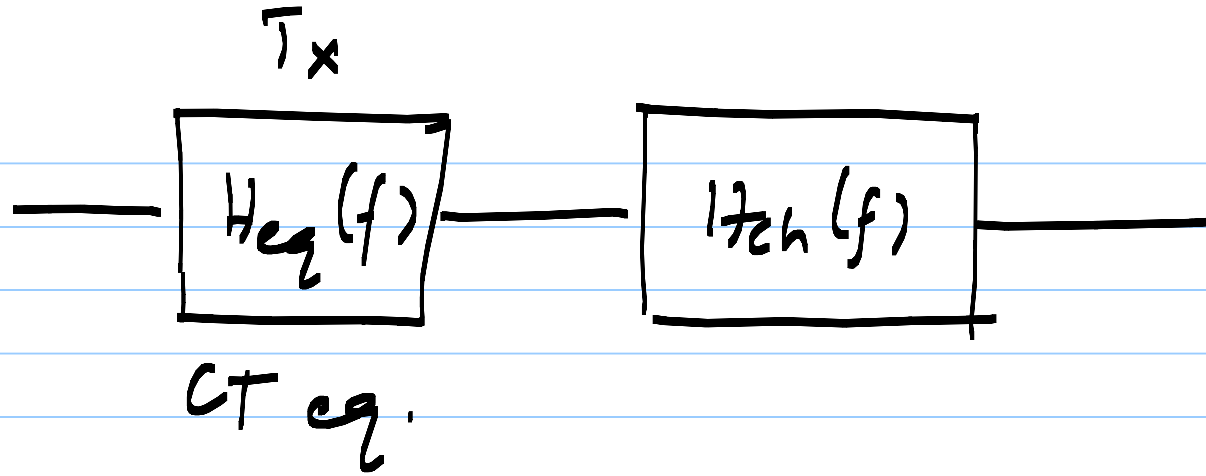
R_x CTLE: Independent of clock recovery

Periodic @ $0.5f_0$

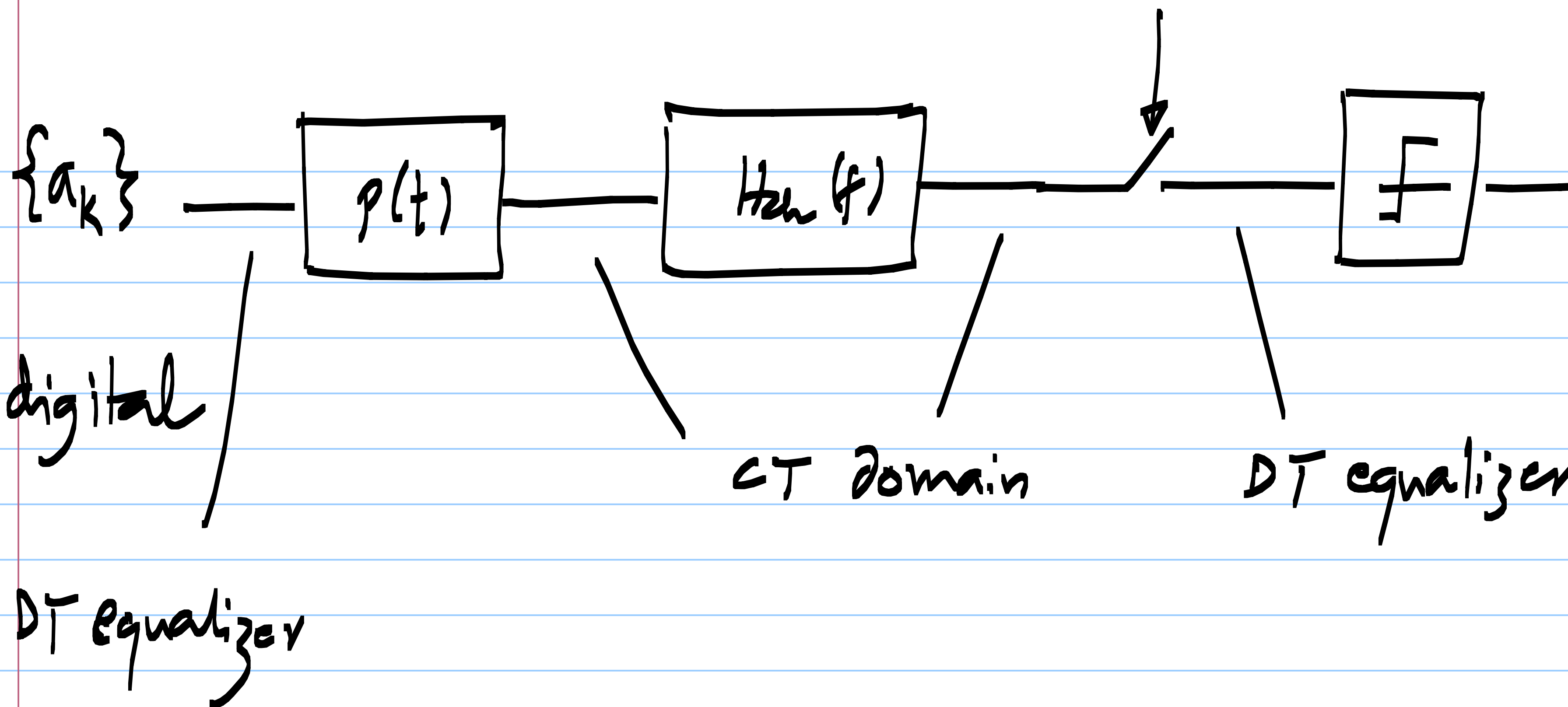
$0.5f_0$ and odd harmonics

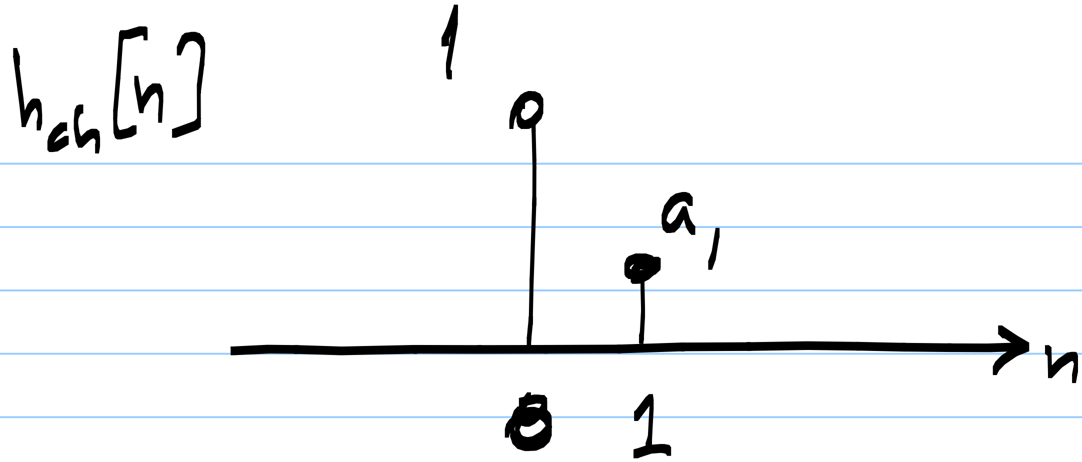
$H_{ch}(0.5f_0)$

~ loss to be compensated at $0.5f_0$



Tx
Heq(f)
Hch(f)
CT eq.

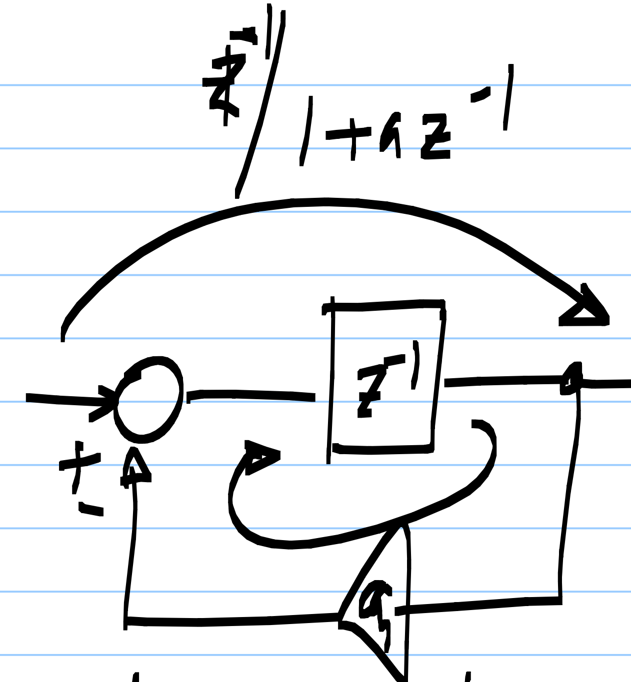

{a_k}
p(t)
H_ch(f)
F
digital
DT equalizer
CT domain
DT equalizer



$$H_{ch}(z) = 1 + a_1 z^{-1}$$

$$H_{ch}(z) \cdot H_{eq}(z) = 1$$

$$H_{eq}(z) = \frac{1}{1 + a_1 z^{-1}}$$ IIR



Feedback has to arrive within 1 cycle.

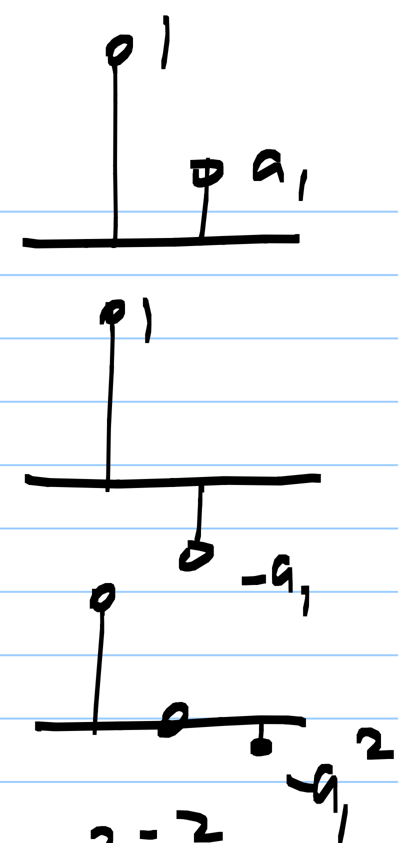
$$H_{ch}(z) \cdot H_{eq}(z) \simeq 1$$

$$H_{eq} = \frac{1}{1 + a_1 z^{-1}} = 1 - a_1 z^{-1} + \dots$$

$$\boxed{H_{eq}(z) = 1 - a_1 z^{-1}}$$

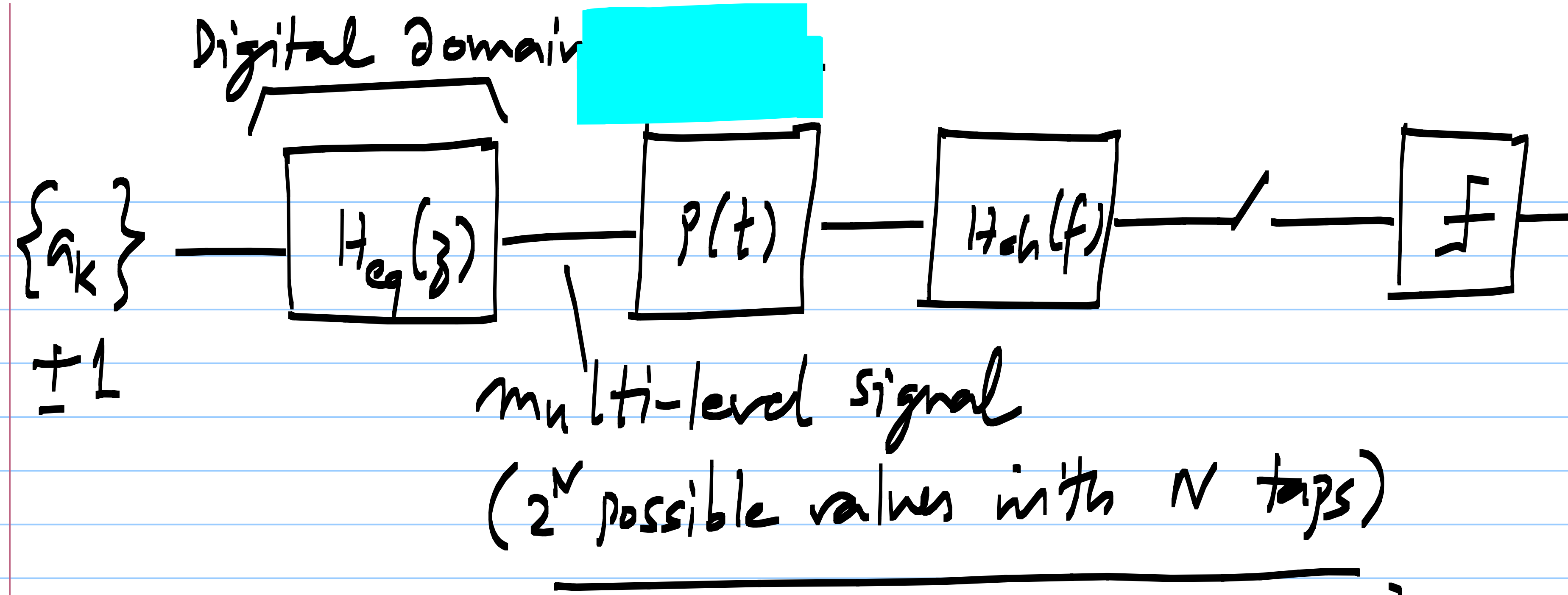
$$H_{ch} \cdot H_{eq} = (1 + a_1 z^{-1})(1 - a_1 z^{-1}) = 1 - \underbrace{a_1^2 z^{-2}}$$

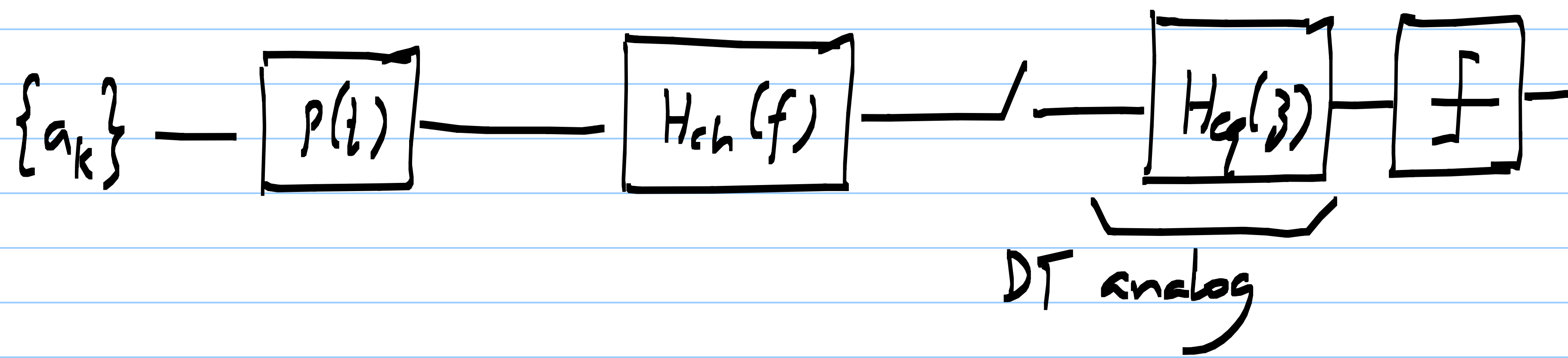
1

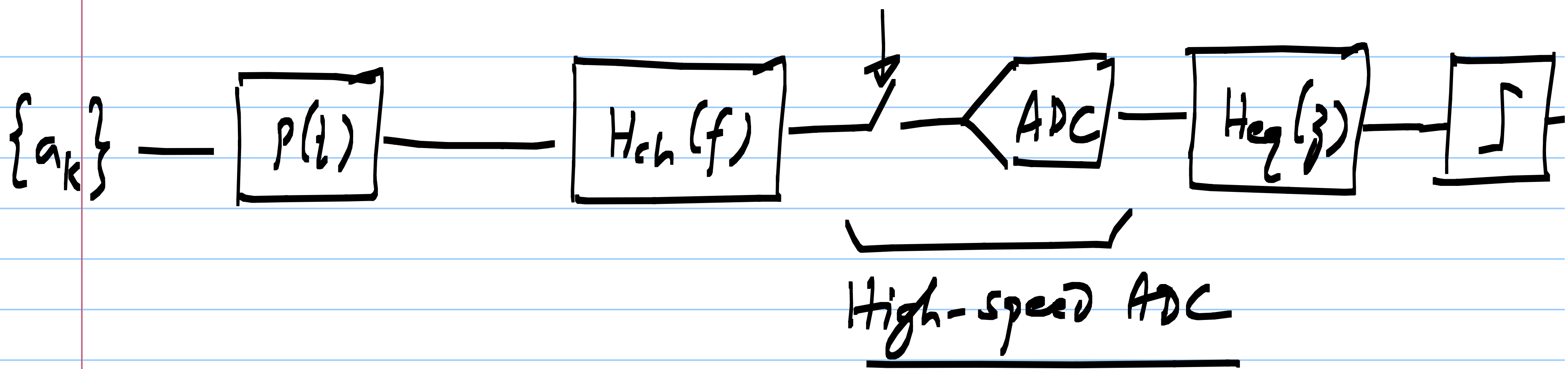


DT equalization:

* FIR realization preferred
  - Difficult to close the fb loop @ high frequencies
* Make the combined impulse response close to an impulse

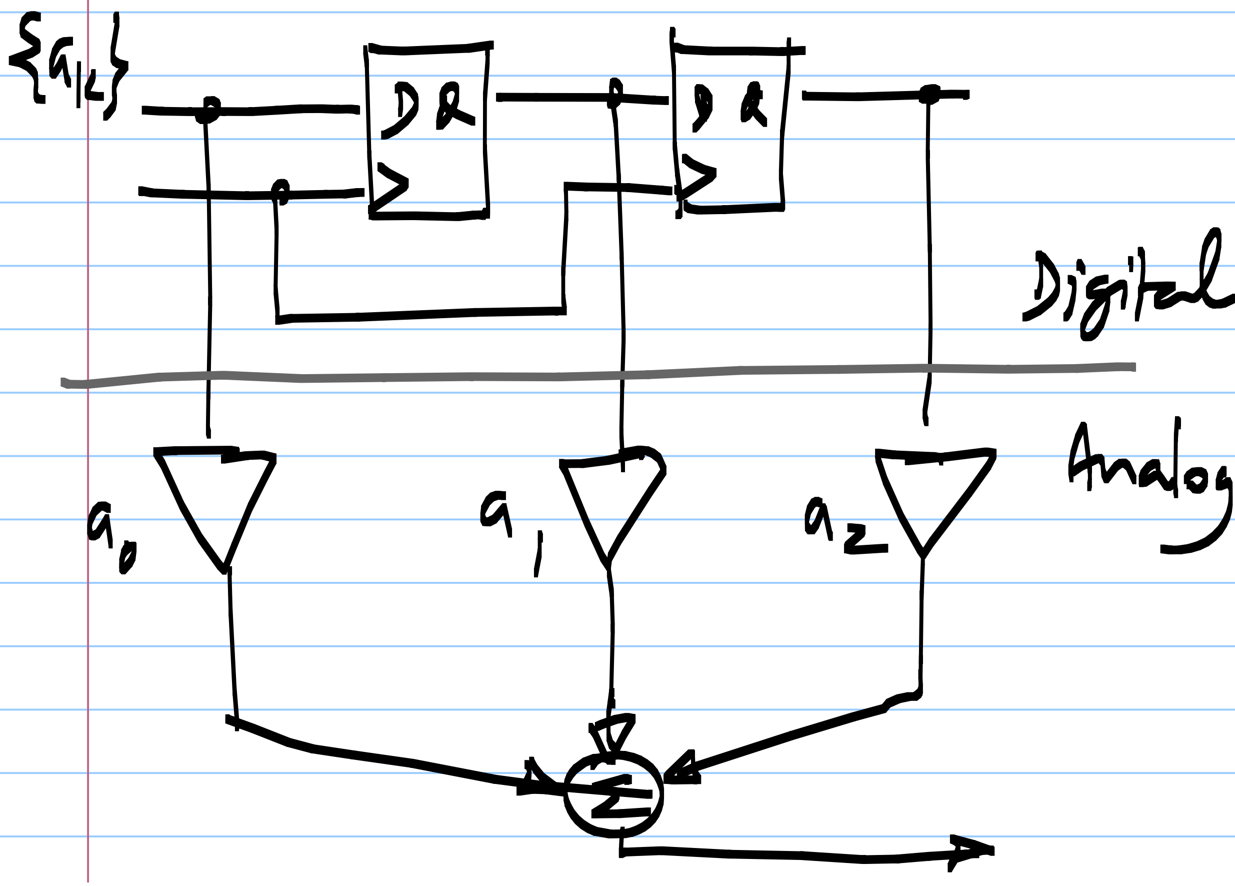

Digital domain
{a_k}
±1
H_eq(z)
p(t)
H_ch(f)
multi-level signal
(2^N possible values with N taps)


{a_k}
p(t)
H_ch(f)
H_eq(z)
DT analog

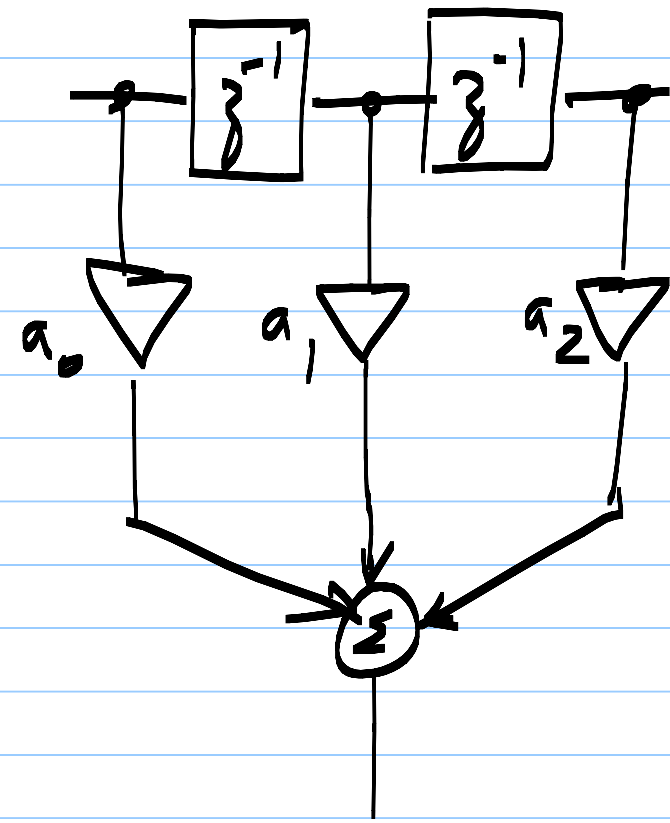

{a_k}
p(t)
H_ch(f)
ADC
H_eq(z)
High-speed ADC

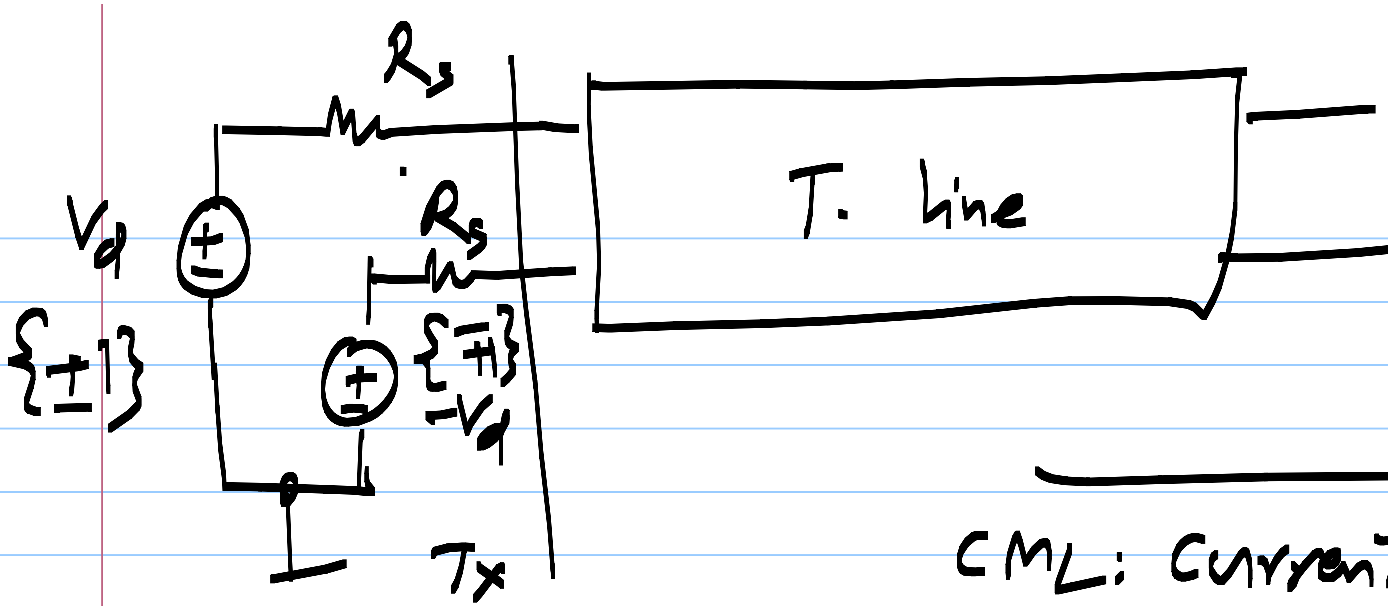
Semi-digital Tx equalizer

Input: digital

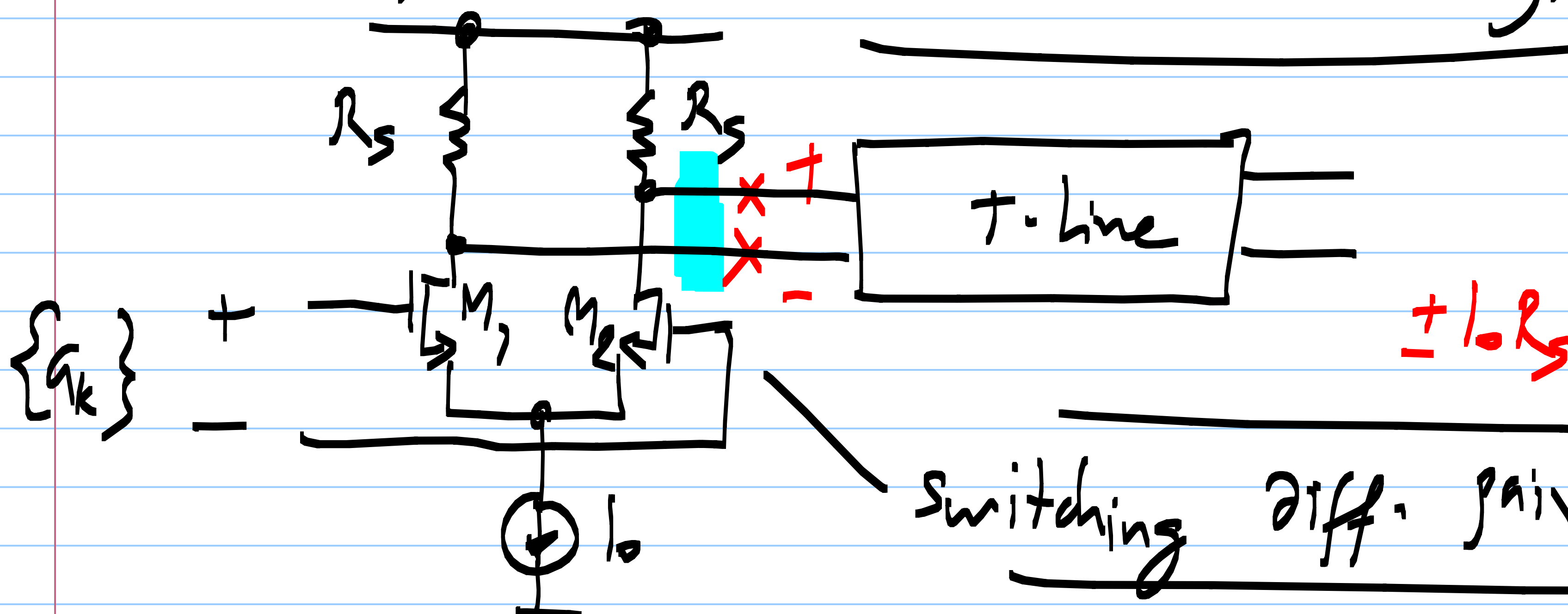


FIR:





CML: current-mode logic

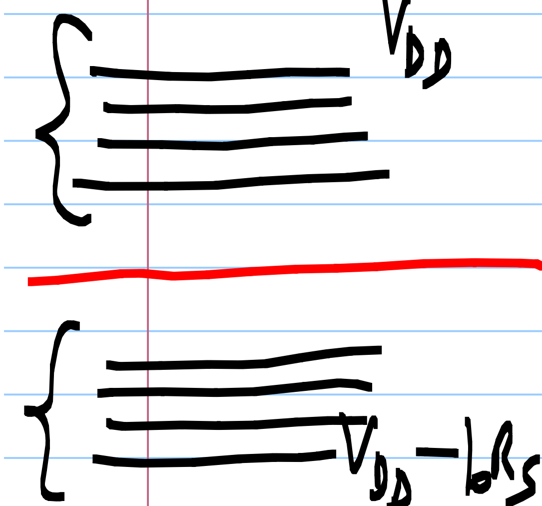


switching diff. pair

$a_{-1} z + a_0 + a_1 z^{-1}$

PRECURSOR — CURSOR

+1 Tx

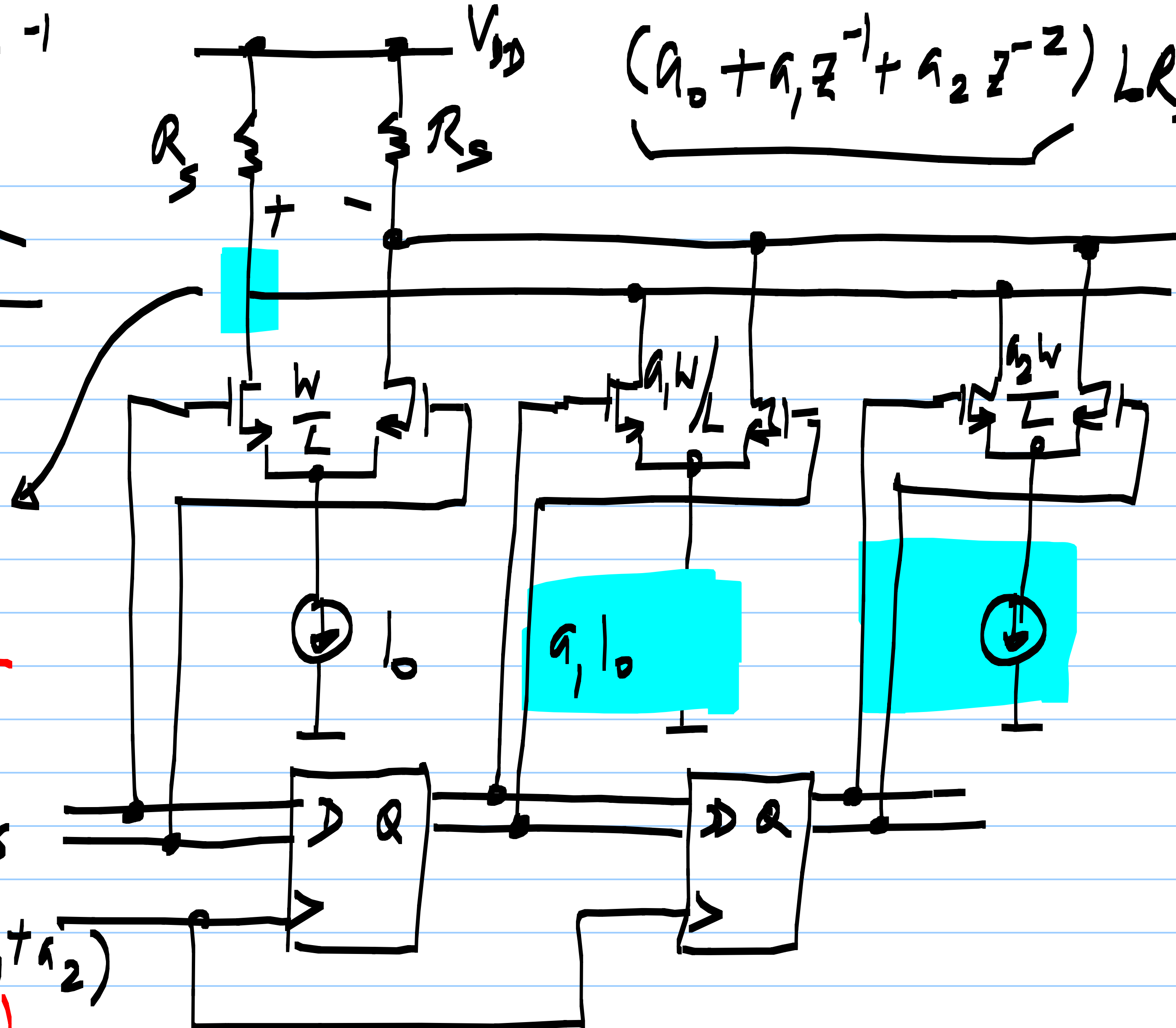


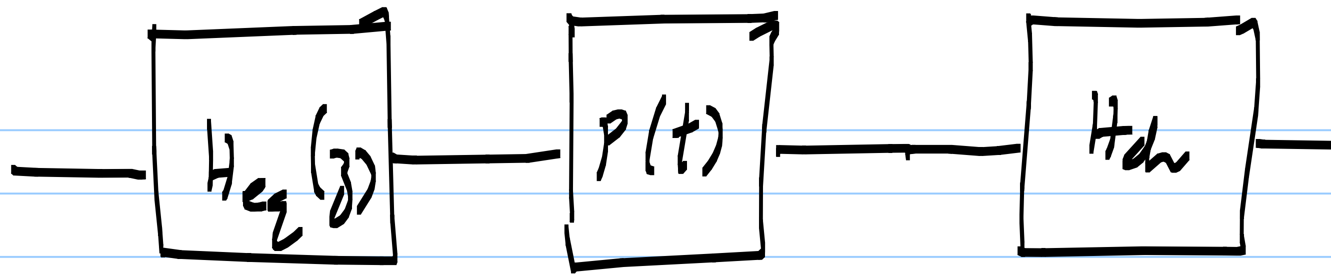
-1

$(1 + a_1 + a_2)$

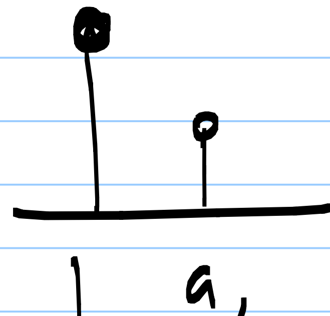
$V_{DD} - \frac{I_0 R_s}{2}(1 + a_1 + a_2)$

$(a_0 + a_1 z^{-1} + a_2 z^{-2}) I_0 R_s$

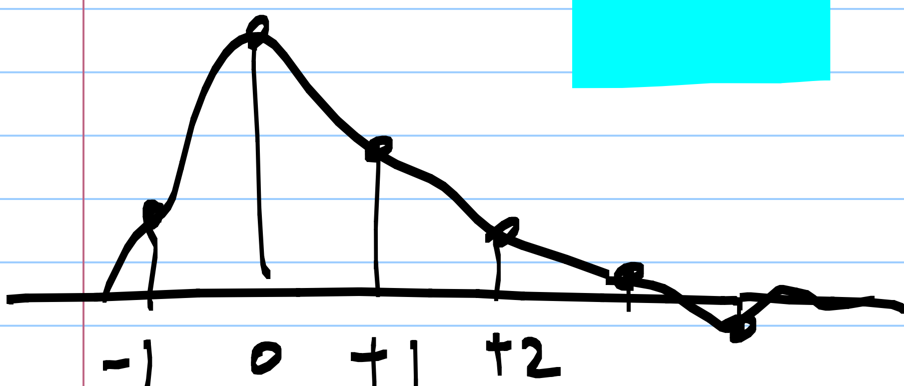


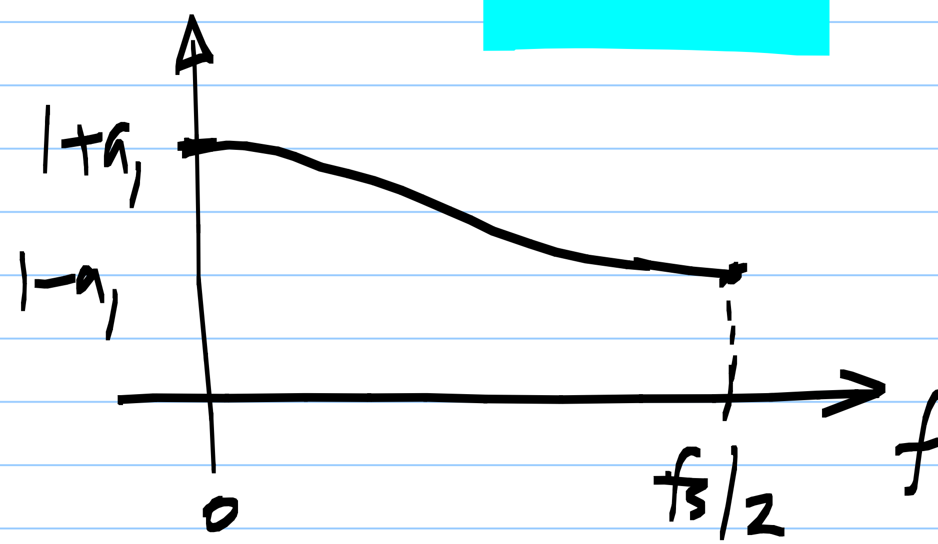


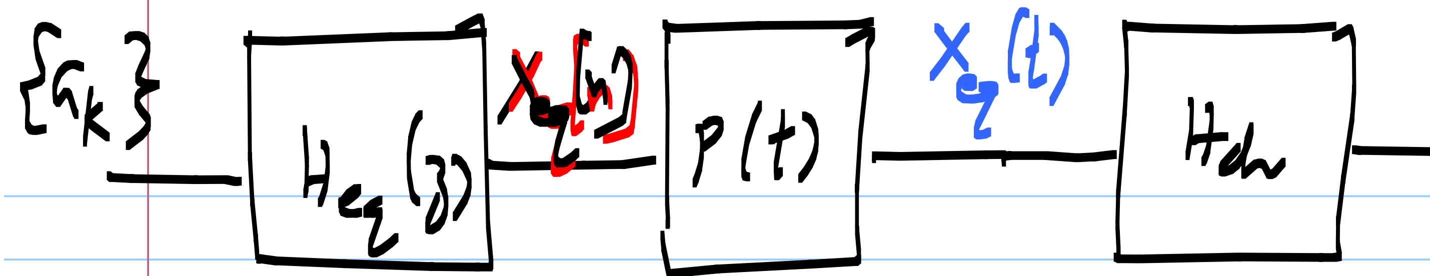
$h_{ch}[n] =$

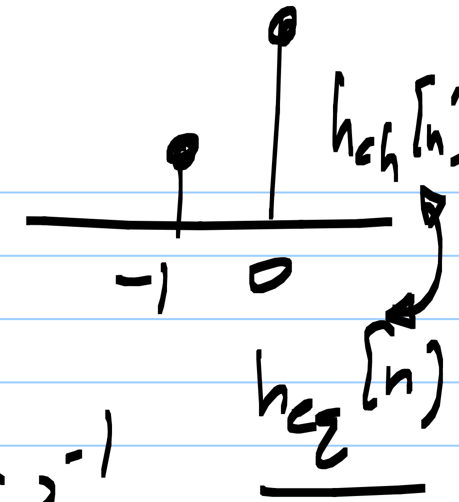


$H_{ch}(z) = 1 + a_1 z^{-1}$

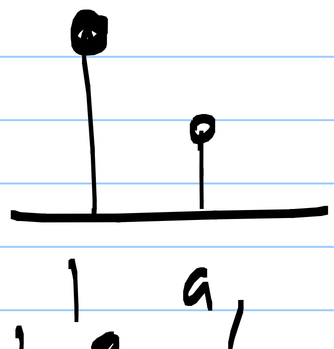






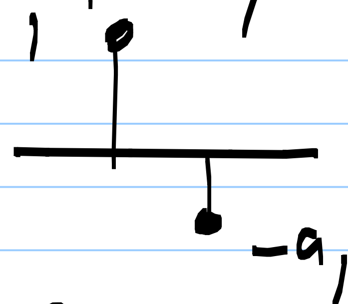


$h_{ch}[n] =$

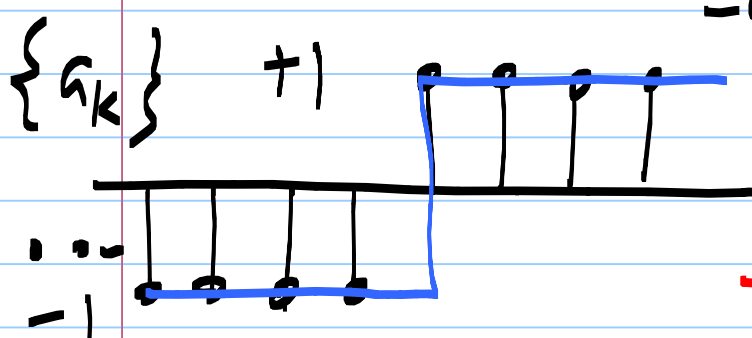


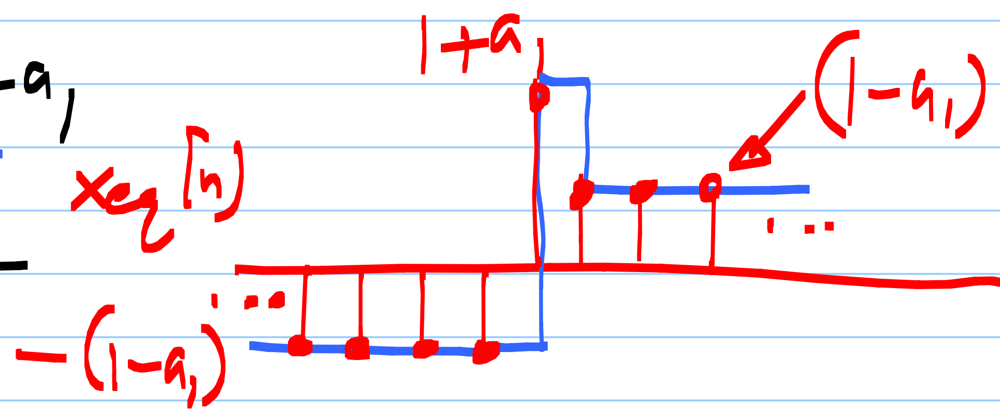
$$H_{ch}(z) = 1 + a_1 z^{-1}$$

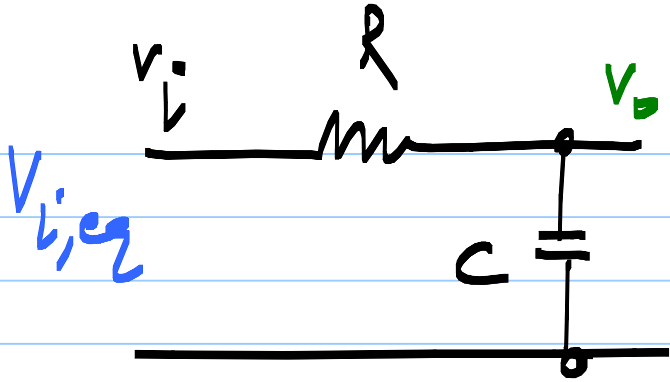
$h_{eq}[n] =$

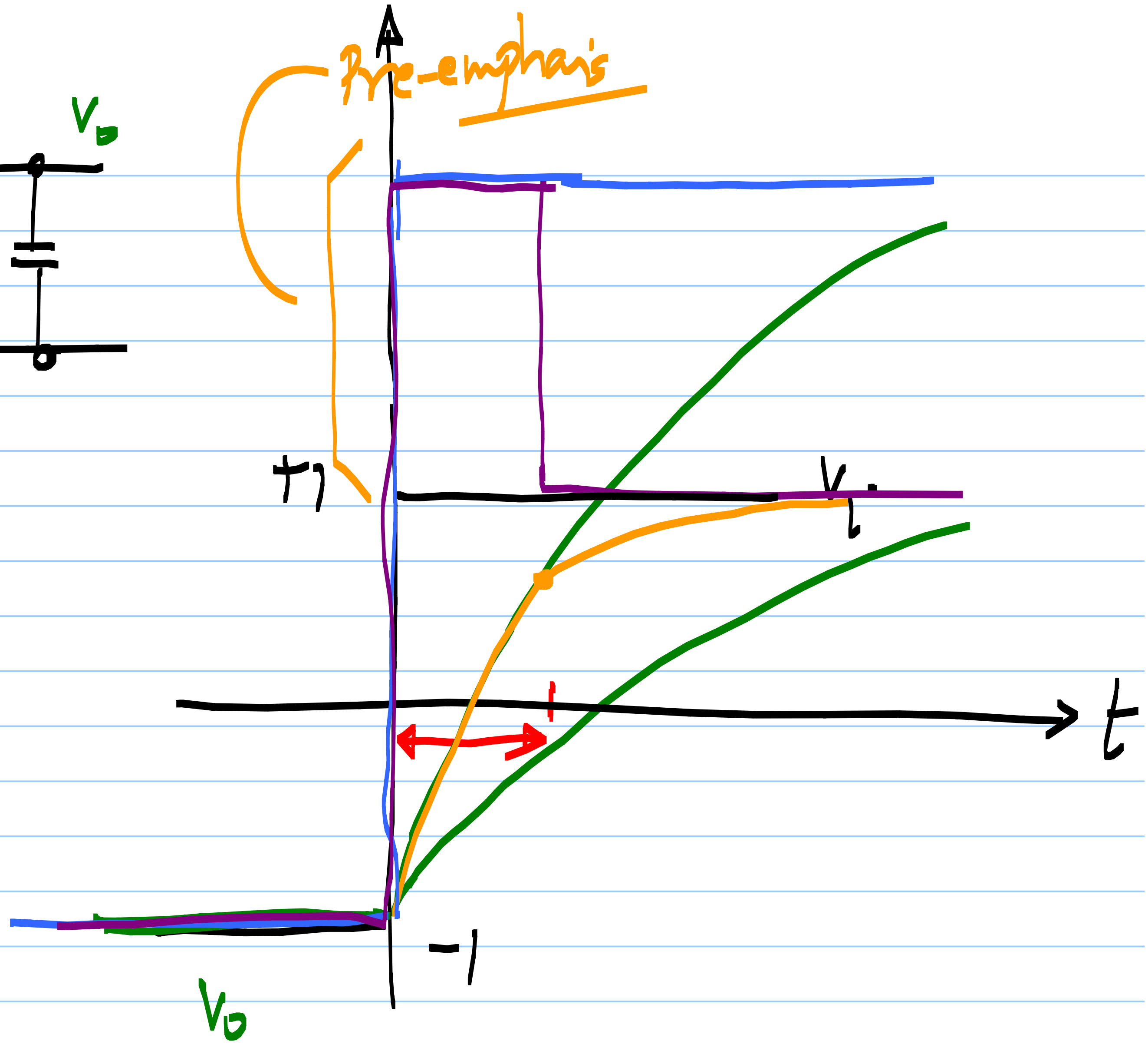


$$H_{eq}(z) = 1 - a_1 z^{-1}$$






v_i
R
v_o
C
V_i,eq


Pre-emphasis
1
v_i
t
-1
v_o