EE5390: Analog Integrated Circuit Design; HW6

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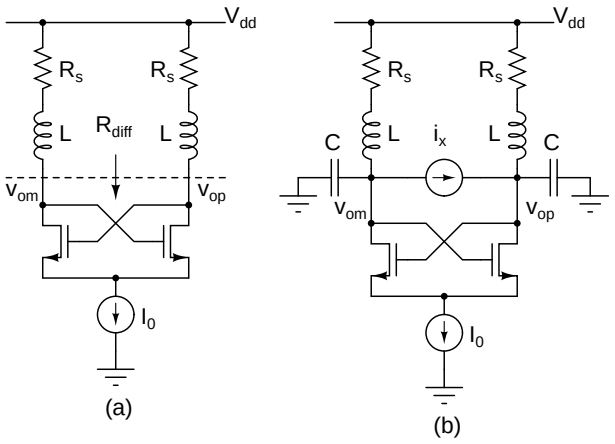

Figure 1:

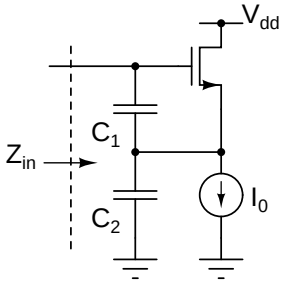

Figure 2:

1. Calculate the current flowing in each transistor in Fig. 1(a) in the quiescent condition. Calculate the small signal differential resistance R_{out} looking into the drains of the two transistors.

   In Fig. 1(b), calculate $(v_{op} - v_{om})/i_x$. What is the condition for this to be infinity? What is the frequency at which this happens?

2. Calculate the input impedance Z_{in} in Fig. 2. Is there anything special about it? Model the transistor using only its g_m.

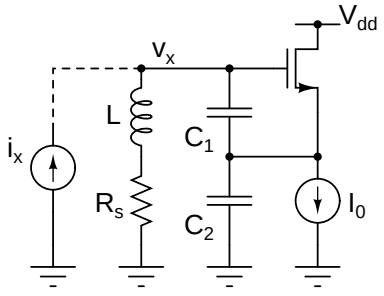

Figure 3:

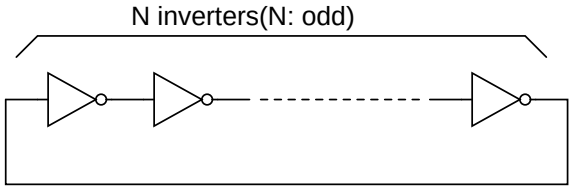

Figure 4:

3. Calculate the small signal impedance v_x/i_x. What is the condition for this to be infinity? What is the frequency at which this happens? Model the transistor using only its g_m.

4. In Fig. 4, assume that all nodes are at the self bias voltage of the inverter. Model the small signal gain of each inverter as $A_0/(1 + s/p_1)$ and calculate the condition for instability (i.e. when the loop gain becomes -1). Hint: Among the roots of -1, pick the one which satisfies the above for the lowest value of A_0.