EE5390: Analog Integrated Circuit Design; Assignment 7

Nagendra Krishnapura (nagendra@iitm.ac.in)

due on

0.18 μm technology parameters: $V_{Tn} = 0.5\,\text{V}$; $V_{Tp} = 0.5\,\text{V}$; $K_n = 300\ \mu\text{A}/V^2$; $K_p = 75\ \mu\text{A}/V^2$; $A_{VT} = 3.5\,mV\ \mu\text{m}$; $A_\beta = 1\%\,\mu\text{m}$; $V_{dd} = 1.8\,\text{V}$; $L_{min} = 0.18\ \mu\text{m}$, $W_{min} = 0.24\ \mu\text{m}$; Ignore body effect unless mentioned otherwise. Ignore 1/f noise unless mentioned otherwise.

1. **Bandgap reference**: Bias a 1x sized diode connected PNP[1] at 10 μA as shown in Fig. 1(a) and sweep the temperature from 0 to 100°C. Determine dV_{BE}/dT at 27°C.

   Design the bandgap shown in Fig. 1(c). Choose R_1 for a quiescent current of 10 μA and R_2 to get zero temperature coefficient at V_{bg}. Choose $R_3 = R_2$. What is the role of R_3? Simulate the bandgap reference with the model of a single stage opamp designed in the previous assignment (Fig. 1(b)-model the gm, and the pole zero doublet). Choose C_c for ringing $\leq$ 10%. Test the bandgap reference by sweeping the temperature from 0 to 100°C and plot V_{bg}. Test the transient response by applying a 1 uA pulse to the output of the opamp. Adjust the values of R_1, R_2, $R_3\,(= R_2)$ if necessary to get zero TC at 27°C.

   Modify the circuit as in Fig. 1(d). How should V_x, V_y, and V_{bg} change? What is the purpose of this modification? Resimulate with the opamp model as before and test the temperature sensitivity, transient response and the loop gain.

   Substitute the differential pair opamp designed in the previous assignment and simulate the temperature sensitivity of V_{bg} and the transient response to a current step at the output.

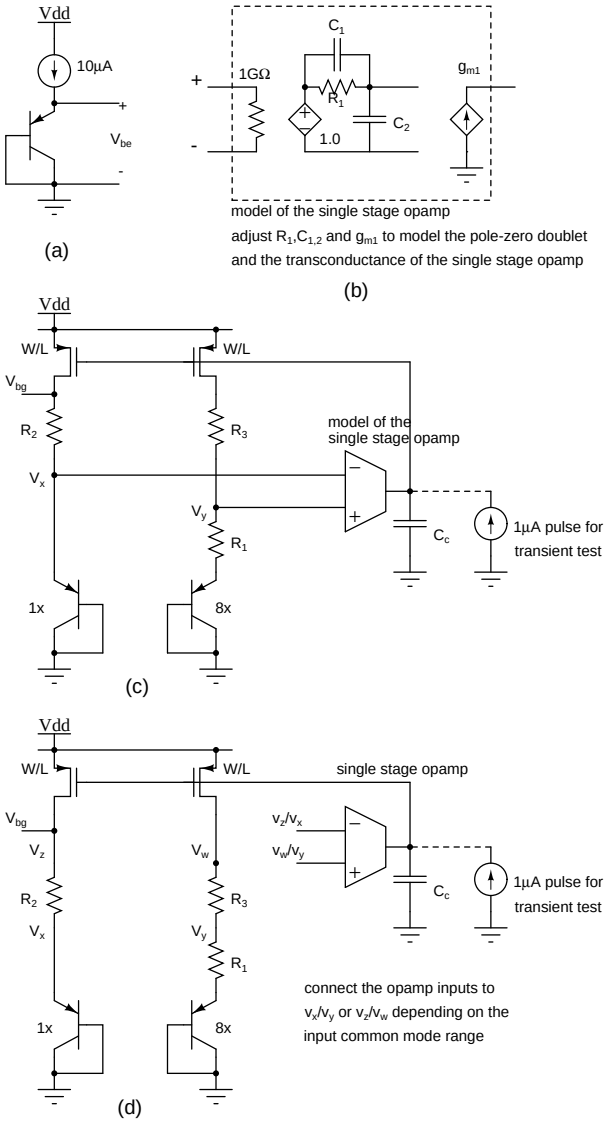

Figure 1: Bandgap reference

2. **Sample and hold**: Design the sample and hold circuit in Fig. 2 using the fully differential folded cascode opamp designed above. Use ideal switches with

[1] Use the model `ideal_pnp` in `ideal_diode.lib`

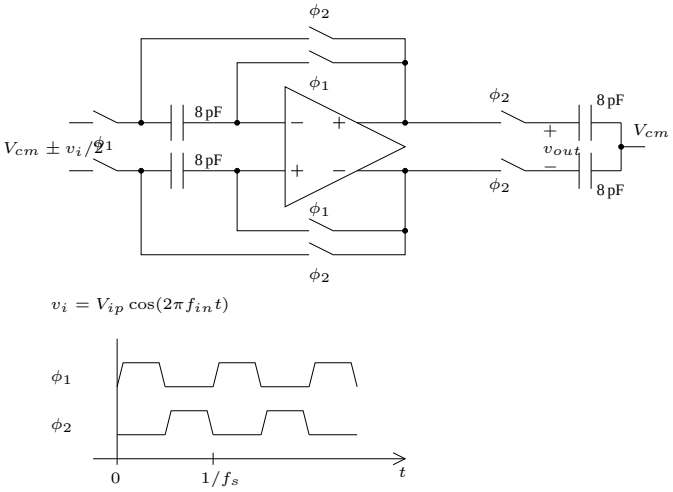

Figure 2: Sample and hold circuit

$1\,\mathrm{k}\Omega$ on resistance. Use $f_s = 4\,\mathrm{MHz}$ and $f_{in} = \{1/4, 9/4\}\,\mathrm{MHz}$ (sinusoidal input with 1.6 Vppd[2] amplitude) and plot the output waveforms. Provide a plot that shows the settling behavior of the opamp.

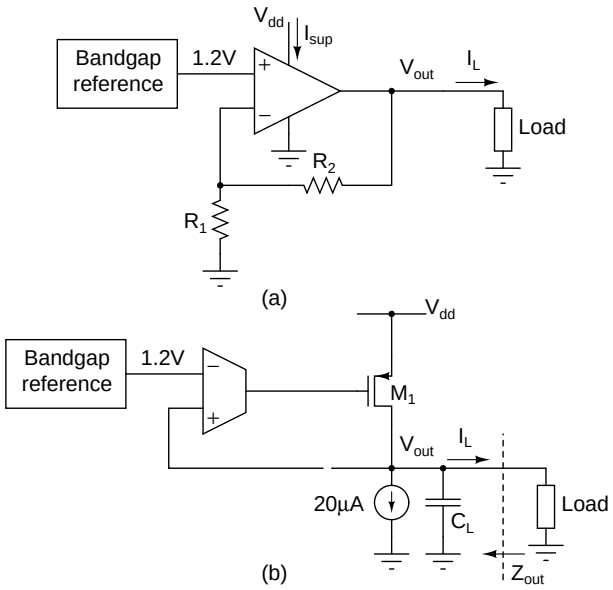

Figure 3: Low dropout regulator

3. **Low dropout regulator (LDO)**: A voltager regulator is nothing but a noninverting amplifier whose input is the bandgap voltage from a reference. In Fig. 3(a), the output voltage is $(R_2/R_1)V_{bg}$. By making R_2 variable, one can get a variable voltage output.

   - The output impedance should be very low: This is accomplished by realizing a very high loop gain over as wide a bandwidth as possible.
   - The efficiency ($(V_{out}I_L)/(V_{dd}I_{sup})$) should be very high: For this, the current $I_{sup} - IL$ consumed by the circuit should be minimized (This makes it hard to satisfy the previous condition). The "dropout" $V_{dd} - Vout$ should be minimized.
   - Usually only a positive I_L needs to be driven. The output voltage is constant over time. These are departures from conventional amplifiers.

   Fig. 3(b) shows a "pass transistor" M_1 enclosed in a feedback loop. For simplicity, a unity gain case is shown. M_1 should have a high enough W/L to remain in saturation with the desired dropout and the highest output current. Miller compensation around M_1 is usually not used because it severely compromises power supply rejection (Incremental voltage gain from V_{dd} to the output voltage).

   Use the model in Fig. 1(b) for the single stage opamp. Use a $50\,\mu$A quiescent current in M_1. Adjust the width (with minimum length) of M_1 for a dropout of 300 mV with a 50 mA current. You can use a 1.2V voltage source in place of the bandgap reference. Compensate the loop using a load capacitor C_L for a phase margin of 45° at $I_L = 0$ and $I_L = 50\,\mathrm{mA}$ and choose the higher one. Do the following (except the last one) for two cases ($I_L = 0$ and $I_L = 50\,\mathrm{mA}$—you can use a current source for the load):

   (a) Vary V_{dd} from 1.4 V to 1.8 V and plot V_{out}

   (b) Plot Z_{out} from 1 kHz to 10 MHz

   (c) Plot the transfer function from V_{dd} to V_{out} from 1 kHz to 10 MHz

   (d) Plot the small signal step response for a 10 μA step in the output current

   (e) Plot the large signal step response (I_L switching from zero to 50 mA and 50 mA to zero)

[2] Vppd: volts, peak-peak differential