EE5390: Analog Integrated Circuit Design; HW6

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0.18 μm technology parameters: $V_{Tn} = 0.5$ V; $V_{Tp} = 0.5$ V; $K_n = 300\ \mu A/V^2$; $K_p = 75\ \mu A/V^2$; $A_{VT} = 3.5\,mV\,\mu$m; $A_\beta = 1\%\,\mu$m; $V_{dd} = 1.8$ V; $L_{min} = 0.18\ \mu$m, $W_{min} = 0.24\ \mu$m; Ignore body effect unless mentioned otherwise.
For all MOS transistors, use $A_d = A_s = 2WL_{min}$; and $P_d = P_s = 2(W + 2L_{min})$

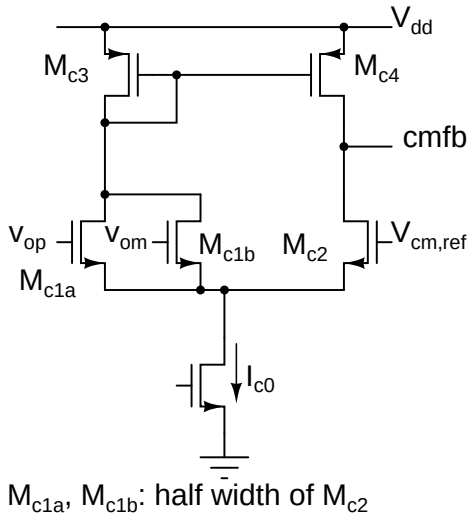

Figure 1: Common mode feedback amplifier for the single stage opamp

1. **Fully differential single stage opamp:** Turn the single stage opamp designed in the previous assignment into a fully differential one by adding common mode feedback. Use the common mode feedback circuit shown in Fig. 1. Make I_{c0} equal to half the tail current in the main differential pair. Choose the sizes of M_{c1-c4} appropriately. Choose the common mode reference to maximize the output swing of the differential pair.

   Show the schematic with operating points, differential magnitude and phase response of the opamp, and common mode loop gain magnitude and phase.

2. **Fully differential two stage opamp:** For this problem, use a pMOS input pair if your roll number is odd and an nMOS input pair if your roll number is even (same as in the single stage case).

   Design a fully differential two stage opamp with a dc gain of at least 1000. The unity gain frequency of the opamp should be 100 MHz with $R_L = 4\,kohm$, $C_L = 2$ pF (connected from each output node to ground). Use an appropriately scaled version of the single stage opamp you designed earlier and add a second stage to it. Use miller compensation with a zero cancelling resistor. Add a single common mode stage around both stages. The phase margin of the opamp's response and the common mode feedback loop gain should be 45°. Scale the CMFB amplifier to obtain the highest $\omega_{u,loop,CM}$ with this phase margin.

   Report the following and show simulation results where appropriate. Tabulate the results neatly as in a data sheet.

   (a) Differential loop gain-magnitude and phase

   (b) Differential closed loop gain-magnitude and phase

   (c) Common mode loop gain-magnitude and phase

   (d) Transient response of the unity gain inverting amplifier with a 0.2 V differential step (use 0.1 ns rise/fall times).

   (e) Transient response of the unity gain inverting amplifier with a 0.1 V common mode step (use 0.1 ns rise/fall times).

(f) Input referred noise spectral density-identify 1/f noise corner. Show relative contributions from different devices at 10 MHz.

(g) Input referred offset (For this, ignore current factor mismatch; Calculate σ_{VT} from the sizes, and use g_m values from the operating point; You can assume $g_m \gg g_{ds}$)

(h) Power consumption

(i) Show a schematic with all sizes and operating points (g_m, g_{ds}, V_{GS}-V_T, I_D) of all transistors and the node voltages.

Do not use an ideal current source in the tail. You can use one ideal reference current source of 1/10$^{\text{th}}$ the tail current for bias generation. Design the bias generator block that generates bias currents and voltages required in the opamp.

Try to determine as many parameters as possible from the specifications and choose sensible starting points for the others. You can assume a gate overdrive of 200 mV in your initial calculations.

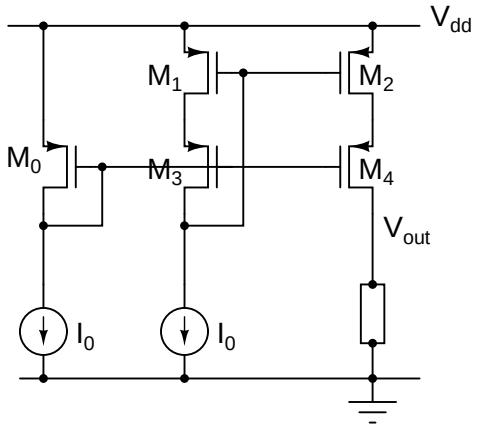

Figure 2: Cascode current source

3. Fig. 2 shows a cascode current source $M_{2,4}$ biased from $M_{0,1,3}$. M_1 and M_3 have an aspect ratio W/L. Determine the sizes of $M_{0,2,4}$ so that the load current is nI_0 and the output compliance (of V_{out}) is maximized.

4. Fig. 3 shows a common drain amplifier. Evaluate the small signal gain v_o/v_s and the output resistance

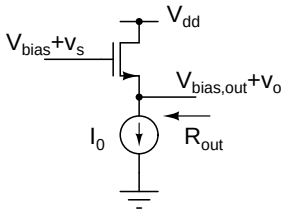

Figure 3: Common drain amplifier

R_{out} including body effect (i.e. model the transistor using g_m and g_{mb} assume $g_{ds} = 0$).

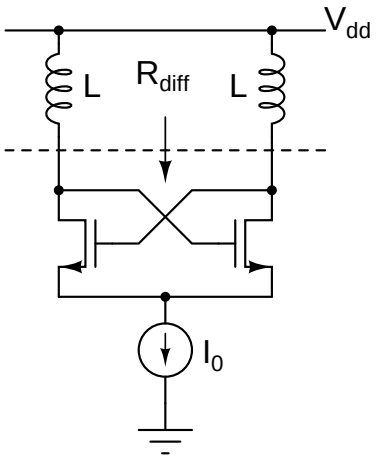

Figure 4:

5. Calculate the current flowing in each transistor in Fig. 4 in the quiescent condition. Calculate the small signal differential resistance R_{out} looking into the drains of the two transistors.

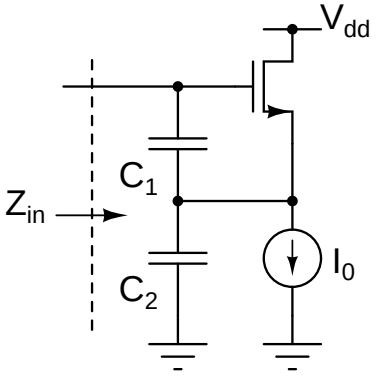

Figure 5:

6. Calculate the input impedance Z_{in} in Fig. 5. Is there

anything special about it? Model the transistor using only its g_m.

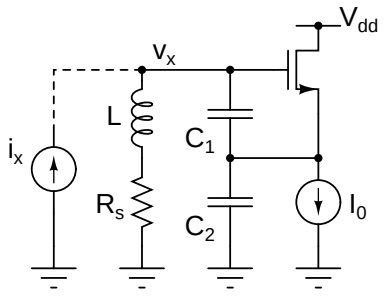

Figure 6:

7. Calculate the small signal impedance v_x/i_x. What is the condition for this to be infinity? Model the transistor using only its g_m.