EE5390: Analog Integrated Circuit Design; HW5

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0.18 μm technology parameters: $V_{Tn} = 0.5\,\text{V}$; $V_{Tp} = 0.5\,\text{V}$; $K_n = 300\ \mu\text{A}/V^2$; $K_p = 75\ \mu\text{A}/V^2$; $A_{VT} = 3.5\,mV\,\mu$m; $A_\beta = 1\%\,\mu$m; $V_{dd} = 1.8\,\text{V}$; $L_{min} = 0.18\ \mu$m, $W_{min} = 0.24\ \mu$m; Ignore body effect unless mentioned otherwise.

For all MOS transistors, use $A_d = A_s = 2WL_{min}$; and $P_d = P_s = 2(W + 2L_{min})$

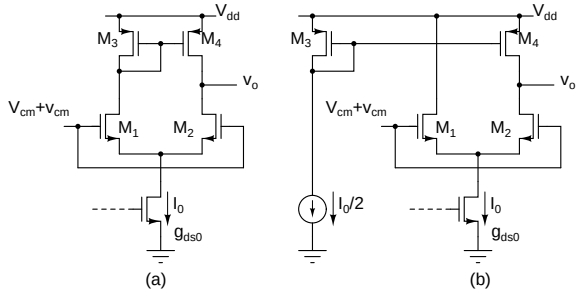

Figure 1:

1. The common mode gain of a differential amplifier is measured by applying a small signal common mode input v_{cm} as shown in Fig. 1. Fig. 1(a) has a current mirror load and Fig. 1(b) has a current source load which is independently biased. What is the common mode gain of these two configurations? Express the answer in terms of the small signal parameters of: M_0 (g_{m0}, g_{ds0}), $M_{1,2}$ (g_{m0}, $g_{ds1} = \infty$), $M_{3,4}$ (g_{m3}, g_{ds3})

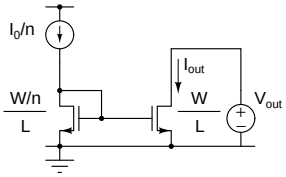

Figure 2:

2. You are required to design a current mirror that can operate with an output voltage V_{out} and deliver a current I_{out} (Fig. 2). What operating conditions will you choose for the devices to minimize the output noise? (consider only the thermal noise spectral density). You try to minimize the reference branch current by scaling it down by a factor of n. What is its implication on the output noise?

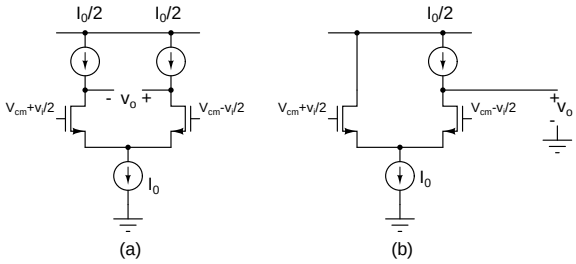

Figure 3:

3. Determine the small signal dc gains of the two amplifiers in Fig. 3. The transistors can be modeled using g_m and g_{ds}. Explain the results.

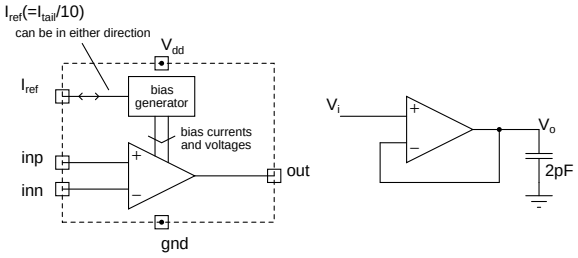

Figure 4:

4. For this problem, use a pMOS input pair if your roll number is odd and an nMOS input pair if your roll number is even.

Design a single stage single ended opamp with a dc gain of 50 using an nMOS differential pair. The application is a unity gain buffer with 0.5 Vpp (± 0.25 V around the common mode) swing. The unity gain buffer should have a 3 dB bandwidth of 100 MHz, with $C_L = 2$ pF. All parasitic poles and zeros should be at at least twice the unity gain frequency. Report the following and show simulation results where appropriate. Tabulate the results neatly as in a data sheet.

(a) Input common mode range

(b) Output voltage range

(c) A_o, ω_u, and open loop poles/zeros

(d) Closed loop frequency response, poles/zeros

(e) DC sweep of the buffer with input varying from 0 to Vdd

(f) Transient response of the unity gain buffer with a +0.1 V step and a -0.1 V step (use 0.1 ns rise/fall times). Report the slew rate and compare it with the theoretical value. (If you don't see slewing, increase the step amplitude until you do)

(g) Input referred noise spectral density-identify 1/f noise corner if applicable. Show relative contributions from different devices at 10 MHz.

(h) Input referred offset (For this, ignore current factor mismatch; Calculate σ_{VT} from the sizes, and use g_m values from the operating point; You can assume $g_m \gg g_{ds}$)

(i) Power consumption

(j) Show a schematic with all sizes and operating points (g_m, g_{ds}, V_{GS}-V_T, I_D) of all transistors and the node voltages.

Do not use an ideal current source in the tail. You can use one ideal reference current source of 1/10$^{\text{th}}$ the tail current for bias generation (Fig. 4). Design the bias generator block that generates bias currents and voltages required in the opamp.

Try to determine as many parameters as possible from the specifications and choose sensible starting points for the others. You can assume a gate overdrive of 200 mV in your initial calculations. Try to adjust the channel lengths so that g_{ds} contributions from nMOS and pMOS sides are equal (This is not the only possible choice. Other choices may be preferable to optimize other figures of merit-e.g. noise. This is a suggested starting point for simplicity). Choose an appropriate common mode voltage.

Maximize the output voltage swing and reduce the power consumption during the design.

Don't submit the following problems, just try them out.

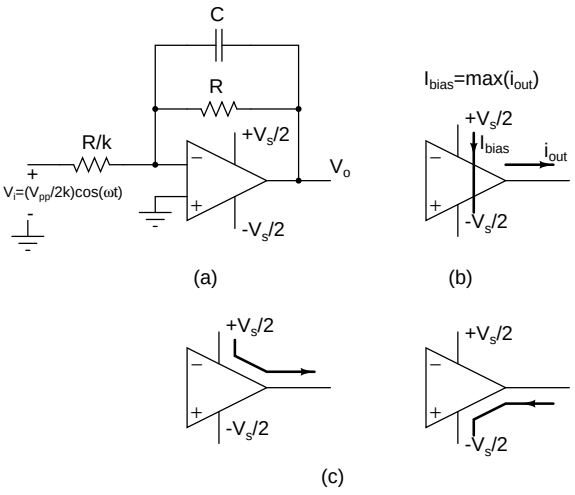

Figure 5:

1. Determine the rms signal, rms noise, signal to noise ratio (as a ratio of mean squared quantities) at the output of Fig. 5. Assume an low frequency input. What is the amplifier's transfer function? The opamp can be either (i) class A (Fig. 5(b)): In this case a constant current I_{bias}, equal to the highest possible output current) is drawn from the amplifier; or (ii) class B (Fig. 5(c)): In this case, currents out of the opamp are drawn from the positive supply and currents into the opamp are pushed into the negative supply. In each case, calculate the power dissipation. Relate the power dissipation to amplifier specifications: gain, bandwidth, and signal to noise ratio.

2. Calculate the small signal tail node voltage v_x in

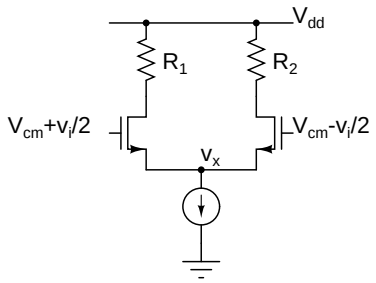

Figure 6:

Fig. 6. v_i is a small signal increment. The transistors can be modeled using g_m and g_{ds}.