EE5390: Analog Integrated Circuit Design; Assignment 4

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0.18 μm technology parameters: $V_{Tn} = 0.5$ V; $V_{Tp} = 0.5$ V; $K_n = 300\ \mu A/V^2$; $K_p = 75\ \mu A/V^2$; $A_{VT} = 3.5\,mV\ \mu$m; $A_\beta = 1\%\,\mu$m; $V_{dd} = 1.8$ V; $L_{min} = 0.18\ \mu$m, $W_{min} = 0.24\ \mu$m; Ignore body effect unless mentioned otherwise.

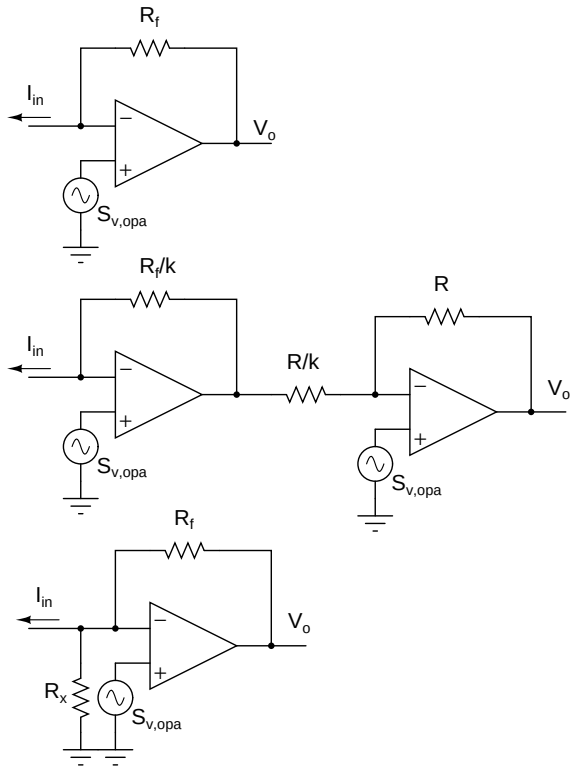

Figure 1:

1. Determine the output noise spectral density and input referred (current) noise spectral density of the transimpedance amplifiers in Fig. 1. The opamp has an input referred voltage noise spectral density of $S_{v,opa}$ V^2/Hz and is otherwise ideal.

2. Design a transimpedance amplifier with a gain of 10 kΩ and the highest possible bandwidth without peaking using an OPA656 opamp. The photodiode has a 5 pF capacitance. Simulate the frequency response, step response (100 μA step input), and input referred and output noise spectral densities. How does the simulated noise compare to analytical calculations? What fraction of noise is contributed by R_f? (The relative contribution of different components can be printed out in the simulator)

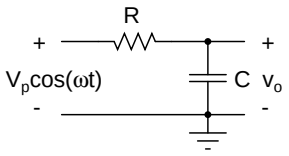

Figure 2:

3. The filter in Fig. 2 is driven by a sinusoid at $\omega = 1/RC$. Calculate the output noise voltage, output signal to noise ratio (ratio of mean squared signal to mean squared noise voltages), and the power dissipated in the circuit. If the impedances of all components are scaled up by a factor α, what happens to the transfer function of the circuit, output noise voltage, output signal to noise ratio, and the power dissipation?

   Derive a relationship between the signal to noise ratio, power dissipation, and the bandwidth of the circuit (in Hz). What tradeoffs does this relationship represent?

4. (For this problem, The minimum usable dimension is $0.3\,\mu$m.) A MOSFET is used as a 200 kΩ resistor (Fig. 3) $V_0 = 0.5\,V$ and v_x is restricted to 0.25 V. The nonlinear part of the current (Difference between the exact expression and its linear approximation) in the resistor should be at most 5%. Cal-

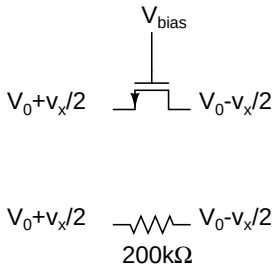

Figure 3:

culate the gate bias V_{bias} and the dimensions of the transistor. If a linear resistive material with a sheet resistance of 10 Ω/sq. is available, what would be its dimensions? What is the motivation for using a transistor instead of a resistive material?

5. Design a 2 pF capacitor using A square nMOS device (drain/source shorted). Plot its capacitance as a function of voltage (0 to 1.8 V). What is the usable voltage range of this capacitor? (For this problem use the process information given in the cadinfo page).

   Repeat the above for a square pMOS device.

   A square Metal1-Metal2 structure.

   A square sandwiched structure with poly, M2, M4 tied together and M1, M3, M5 tied together.

   For the last two structures, determine the bottom plate parasitic capacitance.

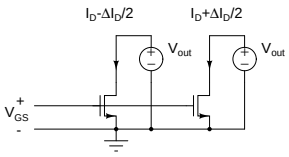

Figure 4:

6. Two transistors carrying a current I_D are required to have a current mismatch $\leq \sigma_{I_D}$ and operate in saturation with an output voltage V_{out} (Fig. 4). Compute the transistor dimensions and its f_T in terms of the mismatch constants A_{VT} and A_β, I_D, σ_{I_D} and V_{out}. Comment on the tradeoffs implied by this relationship.

7. (Repeat this for nMOS and pMOS and compare the results) Bias a transistor with $V_{GS} = V_{DS} = 1.0\,V$ and determine W (with $L = 0.18\,\mu$m) to get a current of 200 μA. Simulate S_{I_D} the noise spectral density of drain current from 100 Hz to 100 MHz.

   Double the length and resize W to get 200 μA, and simulate S_{I_D}. Repeat until $L = 5.76\,\mu$m. Overlay the spectral density plots (log y axis) and identify the $1/f$ noise corners. Plot the $1/f$ noise corners vs. L. Briefly explain the results.

Don't submit the following problems, just try them out. The following are to be simulated. Repeat for pMOS and nMOS.

1. Plot I_D vs. V_{DS} (0 to 1.8 V) for V_{GS} from 0 to 1.5 V in steps of 0.25 V and $V_{BS} = 0$ V. Overlay the plots for $W/L = 3.6\,\mu\text{m}/0.36\,\mu\text{m}$ and $W/L = 36\,\mu\text{m}/3.6\,\mu\text{m}$. Comment on the results.

2. Plot I_D vs. V_{DS} (0 to 1.8 V) for V_{BS} from -1 V to 0 V in steps of 0.25 V and $V_{GS} = 1.5$ V. Overlay the plots for $W/L = 3.6\,\mu\text{m}/0.36\,\mu\text{m}$ and $W/L = 36\,\mu\text{m}/3.6\,\mu\text{m}$. Comment on the results.

3. Plot (log-log) I_D vs. V_{GS} (18 mV to 1.8 V) for $V_{DS} = 1$ V and $V_{BS} = 0$ V. Overlay the plots for $W/L = 3.6\,\mu\text{m}/0.36\,\mu\text{m}$ and $W/L = 36\,\mu\text{m}/3.6\,\mu\text{m}$ and temperatures of $\{0, 27, 100\}$°C. Comment on the results. Calculate the subthreshold slope η. The current in a MOS transistor in the subthreshold region is proportional to $\exp(V_{GS}/\eta V_t)$ where V_t is the thermal voltage.

4. Plot (log-log) I_D vs. V_{BS} (-1.5 V to -15 mV) for $V_{DS} = 1$ V and $V_{GS} = 1$ V. Overlay the plots for $W/L = 3.6\,\mu\text{m}/0.36\,\mu\text{m}$ and $W/L = 36\,\mu\text{m}/3.6\,\mu\text{m}$ and temperatures of $\{0, 27, 100\}$°C. Comment on the results.