EE5390: Analog Integrated Circuit Design; Assignment 1

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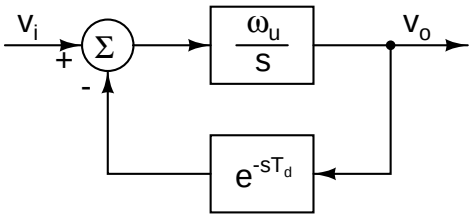

Figure 1: Problem 1

1. For zero input in Fig. 1, will the system admit solutions of the form $v_o(t) = V_p \exp(-\alpha t)\cos(\omega t)$ ($\alpha > 0$)? If so, find out the value of excess loop delay T_d in terms of ω_u and the constraints for α and ω. First do this for $\alpha = 0$ (constant amplitude oscillations) and then for $\alpha = \omega$ and $\alpha = 0.1\omega$. In each case, find out the smallest value of T_d that satisfies the constraints. Plot the natural response in the three cases. What do you infer from this?

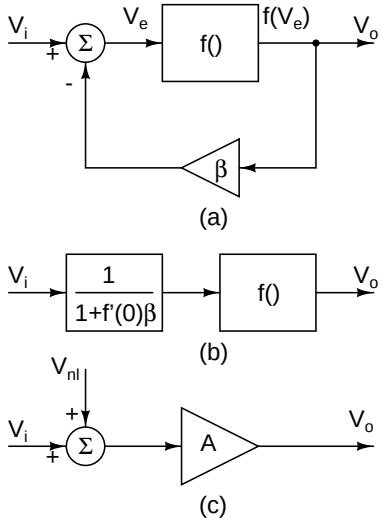

Figure 2: Problem 2

2. Fig. 2(a) shows a nonlinearity f enclosed in a negative feedback loop with a feedback fraction β. Fig. 2(b) shows a nonlinearity f preceded by an attenuation factor. In each case, denote the transfer characteristic of the overall system by g, i.e. $V_o = g(V_i)$ and calculate the first three terms of the Taylor series of g about the operating point of the circuit in terms of f and its derivatives. Assume that $f(0) = 0$.

   Fig. 2(c) shows the linear small signal equivalent circuit from V_i to V_o with an additional input V_{nl}. For the systems in Fig. 2(a) and Fig. 2(b), compute the small signal equivalent gain A and the additional input V_{nl}. What do you infer from the results?

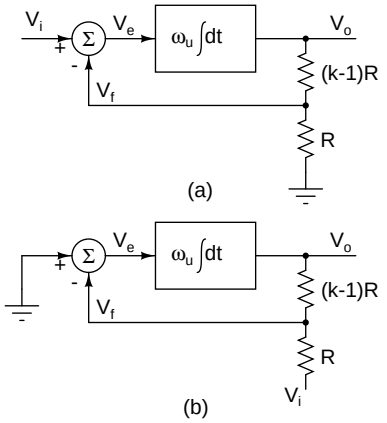

Figure 3: Problem 3

3. Fig. 3(a) shows the amplifier studied in class. Fig. 3(b) shows the same system with the input applied at a different place. Calculate the dc gain, the -3dB bandwidth, and the gain bandwidth product of the system and compare them to the corresponding quantities in Fig. 3(b). Also compare the loop gains. Remark on conventional wisdom such as "constant gain bandwidth product", "closed loop bandwidth =

unity gain frequency/closed loop dc gain". What is the reason for the discrepancy?

Draw an equivalent block diagram of Fig. 3(b) such that the classical form of feedback (sensed error integrated to drive the output) is clearly obvious (Hint: compute the error voltage V_e).

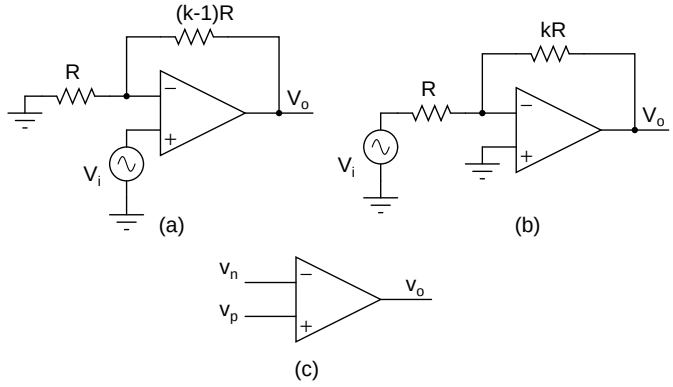

Figure 4: Problem 4

4. Fig. 4(a) and Fig. 4(b) shows amplifiers which realize gains of k and $-k$ respectively with ideal opamps. Compare the following parameters of the two circuits.

   (a) Input resistance

   (b) Bandwidth, assuming that the opamp is modelled as $V_o(s) = (\omega_u/s)(V_p(s) - V_n(s))$

   (c) DC output voltage, assuming that the opamp is modelled as $v_o = A_d(v_p - v_n) + A_{cm}(v_p + v_n)/2$. (Ideally the opamp should respond to only the differential voltage. But, in reality, it responds to the common mode voltage as well.)

   (d) Differential and common mode input voltages of the opamps

   (v_p and v_n are the input voltages of the opamp as shown in Fig. 4(c).)

   Assuming that the sign is unimportant in your application, what would make you choose one over the other? Is there any reason to choose Fig. 4(b) at all?

5. Design inverting and non-inverting amplifers with gains -5 and $+5$ respectively using the opamp OPA656 and ± 6 V supplies. Simulate these amplifiers with 10 MHz sinusoidal inputs of 400 mV peak. Compute the distortion components upto the fifth harmonic and compare the distortion performance of the two amplifiers.

   Plot the differential and common mode inputs of the opamp in the two cases and explain the results using the results from the previous problem.

   When taking the DFT for distortion analysis, ensure that steady state is reached (wait for a sufficiently long time before taking the first point) and that you use an integer number of cycles to avoid spectral leakage (Refer to http://www.ee.iitm.ac.in/∼nagendra/E6316/current/handouts.html or the relevant lecture from EE658 at http://www.ee.iitm.ac.in/∼nagendra/videolectures/)

   OPA656 model is available at http://www.ee.iitm.ac.in/∼nagendra/cadinfo.html