EE539: Analog Integrated Circuit Design; HW7

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For the opamps, **use an nMOS input pair if your roll number is odd** and a **pMOS input pair if your roll number is even**. After you are done with the assignment, compare your results to your friends' designs with same and different input transistor types.

0.18 μm technology parameters: $V_{Tn} = 0.5$ V; $V_{Tp} = 0.5$ V; $K_n = 300\ \mu\text{A}/V^2$; $K_p = 75\ \mu\text{A}/V^2$; $A_{VT} = 3.5\,mV\,\mu$m; $A_\beta = 1\%\,\mu$m; $V_{dd} = 1.8$ V; $L_{min} = 0.18\ \mu$m, $W_{min} = 0.24\ \mu$m; Ignore body effect unless mentioned otherwise. For all MOS transistors, use $A_d = A_s = 2WL_{min}$; and $P_d = P_s = 2(W + 2L_{min})$

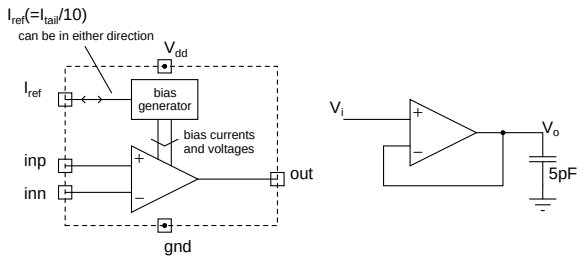

Figure 1:

1. **Simple differential pair**: Design a single stage single ended opamp with a dc gain of 50 using an nMOS differential pair. The application is a unity gain buffer with 0.5 Vpp (± 0.25 V around the common mode) swing. The unity gain buffer should have a 3 dB bandwidth of 100 MHz, with $C_L = 5$ pF. All parasitic poles and zeros should be at at least twice the unity gain frequency. Report the following and show simulation results where appropriate. Tabulate the results neatly as in a data sheet.

   (a) Input common mode range

   (b) Output voltage range

   (c) A_o, ω_u, and open loop polse/zeros

   (d) Closed loop frequency response, poles/zeros

   (e) DC sweep of the buffer with input varying from 0 to Vdd

   (f) Transient response of the unity gain buffer with a +0.1 V step and a -0.1 V step (use 0.1 ns rise/fall times). Report the slew rate and compare it with the theoretical value. (If you don't see slewing, increase the step amplitude until you do)

   (g) Input referred noise spectral density-identify 1/f noise corner if applicable. Show relative contributions from different devices at 10 MHz.

   (h) Input referred offset (For this, ignore current factor mismatch; Calculate σ_{VT} from the sizes, and use g_m values from the operating point; You can assume $g_m \gg g_{ds}$)

   (i) Power consumption

   (j) Show a schematic with all sizes and operating points (g_m, g_{ds}, V_{GS}-V_T, I_D) of all transistors and the node voltages.

Do not use an ideal current source in the tail. You can use one ideal reference current source of 1/10$^{\text{th}}$ the tail current for bias generation (Fig. 1). Design the bias generator block that generates bias currents and voltages required in the opamp.

Try to determine as many parameters as possible from the specifications and choose sensible starting points for the others. Try to adjust the channel lengths so that g_{ds} contributions from nMOS and pMOS sides are equal (This is not the only possible choice. Other choices may be preferable to optimize

other figures of merit-e.g. noise. This is a suggested starting point for simplicity). Choose an appropriate common mode voltage.

Maximize the output voltage swing and reduce the power consumption during the design.

2. **Telescopic cascode amplifier**: Normally you'd design the amplifier starting from specifications. In this case, to make life easier, just take the differential pair above, and add cascode devices. The latter should have the same width as the devices they are used as a cascode for, and minimum length. Design the biasing circuit for the cascode devices to maximize the output swing. Report (a) through (j) above.

3. **Folded cascode amplifier**: Normally you'd design the amplifier starting from specifications. In this case, to make life easier, just take the differential pair above, and add cascode devices. The latter should have the same width as the devices they are used as a cascode for, and minimum length. Design the biasing circuit for the cascode devices to maximize the output swing. The current source at the output of the input differential pair should not contribute more than 25% of the thermal noise. Slew rate limitation due to input and output stages must be the same. Report (a) through (j) above.