EE539: Analog Integrated Circuit Design; HW5

Nagendra Krishnapura (nagendra@iitm.ac.in)

due on 9 Mar. 2008

0.18 μm technology parameters: $V_{Tn} = 0.5$ V; $V_{Tp} = 0.5$ V; $K_n = 300\ \mu A/V^2$; $K_p = 75\ \mu A/V^2$; $A_{VT} = 3.5\,mV\,\mu$m; $A_\beta = 1\%\,\mu$m; $V_{dd} = 1.8$ V; $L_{min} = 0.18\ \mu$m, $W_{min} = 0.24\ \mu$m; Ignore body effect unless mentioned otherwise.

For all MOS transistors, use $A_d = A_s = 2WL_{min}$; and $P_d = P_s = 2(W + 2L_{min})$

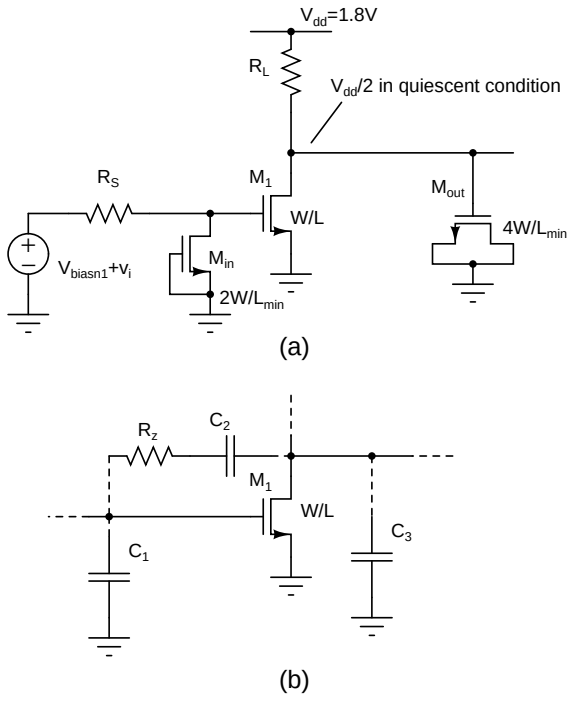

Figure 1: (a) Amplifier, (b) Compensation schemes

1. Common source amplifier design: Design the amplifier in Fig. 1 to have the maximum bandwidth while subject to the following conditions: M_1 should have a $V_{GS} - V_T$ of 150 mV or less; The quiescent output voltage should be 0.9 V. $R_L = 9$ kΩ. R_s = 100 kΩ. g_{ds} of M_1 must contribute less than 5% of the total load conductance. M_{in} and M_{out} represent capacitive loading at the input and the output and their sizes are given in Fig. 1.

   Plot the magnitude and phase response of V_o/V_i, dc transfer characteristics V_o versus V_i, and the noise voltage spectral density referred to the gate of M_1 (i.e. noise from R_s must not be included). If this amplifier is enclosed in a unity feedback loop, will it be stable?

   Compensation: Compensate the above designed amplifier to have a phase margin of 60° in the following ways. Tabulate the relevant component values and the unity gain frequency and explain the results.
   (a) C_1 from the input to ground
   (b) C_3 from the output to ground
   (c) C_2 between the input and the output with $R_z = 0$
   (d) C_2 between the input and the output with $R_z = 1/g_m$

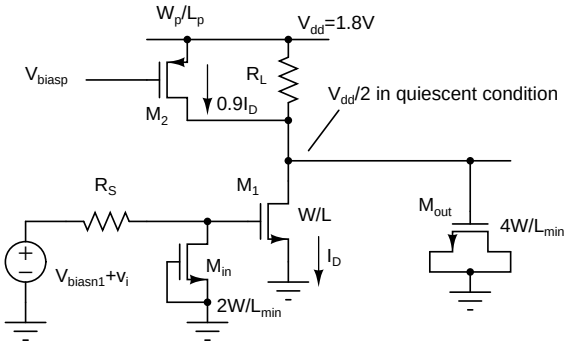

Figure 2:

2. Design the amplifier with an additional pMOS current source (Fig. 2) to have the maximum bandwidth while subject to the following conditions: M_1 and M_2 should have a $V_{GS} - V_T$ of 150 mV or less; The quiescent output voltage should be 0.9 V. I_D

should be the same as in the previous problem. R_s = 100 kΩ. g_{ds} of M_1 and M_2 must in total contribute less than 20% of the total load conductance.

Plot the magnitude and phase response of V_o/V_i, dc transfer characteristics V_o versus V_i, and the noise voltage spectral density referred to the gate of M_1 (i.e. noise from R_s must not be included). If this amplifier is enclosed in a unity feedback loop, will it be stable?

Compensate the amplifier for 60° phase margin using C_2 and $R_z = 1/g_m$. What is the unity gain frequency?

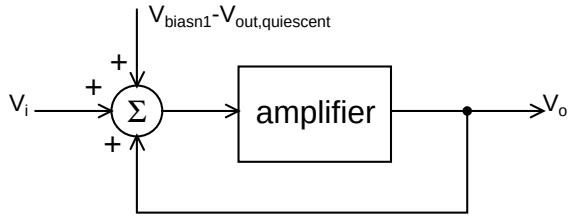

Figure 3:

3. Enclose the amplifiers in Fig. 1 and Fig. 2 (both with compensation using C_2 and $R_z = 0$, $R_z = 1/g_m$) in an ideal unity gain feedback loop as shown in Fig. 3. At the input, add a bias as shown to establish the correct input and output quiescent voltages with $V_i = 0$.

   Determine the frequency response and the step response (for a 100 mV output step). Explain the differences.

   Plot the second and third harmonic distortion with a 1 MHz input sinusoid versus the input amplitude. Start from small values of input amplitude and increase it up to a point where the higher of the distortion components is 40 dB below the fundamental. Explain the results.

4. Frequency compensation using C_2 and $R_z = 1/g_m$ relies on matching a resistance with a transistor's g_m. How would you ensure reliable compensation with this method?

Don't submit the following problems, just try them out.

1. Vary the compensation capacitor in each of the compensation schemes above and observe the frequency response

2. Analytically calculate the poles and zeros. For this, you can use the operating point information of the transistor. Calculate the transfer function analytically. Solve for the poles and zeros numerically, and also using the approximations discussed in class. How good are the approximations?

3. How close is the input referred noise spectral density to $8/3(kT/g_m)$?