

# EE539: Analog Integrated Circuit Design; HW3

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0.18  $\mu\text{m}$  technology parameters:  $V_{Tn} = 0.5\text{ V}$ ;  $V_{Tp} = 0.5\text{ V}$ ;  $K_n = 300\ \mu\text{A}/\text{V}^2$ ;  $K_p = 75\ \mu\text{A}/\text{V}^2$ ;  $A_{VT} = 3.5\text{ mV}\ \mu\text{m}$ ;  $A_\beta = 1\%\ \mu\text{m}$ ;  $V_{dd} = 1.8\text{ V}$ ;  $L_{min} = 0.18\ \mu\text{m}$ ,  $W_{min} = 0.24\ \mu\text{m}$ ; Ignore body effect unless mentioned otherwise.

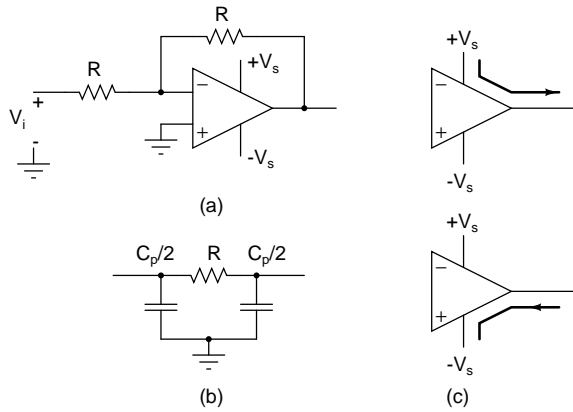


Figure 1:

- The opamp used in Fig. 1(a) has an ideal integrator response  $\omega_u/s$ . The resistors used have a sheet resistance  $R_{sh}$ , a parasitic capacitance per unit area  $C_a$ , and a relative mismatch standard deviation  $\sigma_R = A_R/\sqrt{WL}$ . The parasitic capacitance  $C_p$  is modeled as shown in Fig. 1(b). The opamp is such that current out of the opamp is supplied from the positive supply and current into the opamp is supplied from the negative supply.

Calculate the loop gain  $L(s)$ . Choose  $\omega_u$  to get the highest bandwidth without peaking in the frequency response. What is the closed loop bandwidth of the amplifier in this condition? What is relative gain error  $\sigma_A$ ? Calculate the total power  $P_d$  driven from the power supplies when the input is a sinusoid of peak value  $V_p$ . (Express your answers in terms of resistor

dimensions and process constants.)

Relate the power dissipation  $P_d$ , relative gain error  $\sigma_A$ , and the amplifier bandwidth. What tradeoffs are implied by this relationship?

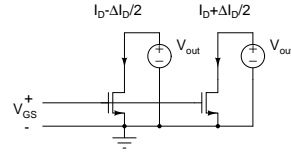


Figure 2:

- Two transistors carrying a current  $I_D$  are required to have a current mismatch  $\leq \sigma_{I_D}$  and operate in saturation with an output voltage  $V_{out}$  (Fig. 2). Compute the transistor dimensions and its  $f_T$  in terms of the mismatch constants  $A_{VT}$  and  $A_\beta$ ,  $I_D$ ,  $\sigma_{I_D}$  and  $V_{out}$ . Comment on the tradeoffs implied by this relationship.

- (Repeat this for nMOS and pMOS and compare the results) Bias a transistor with  $V_{GS} = V_{DS} = 0.8\text{ V}$  and determine  $W$  (with  $L = 0.18\ \mu\text{m}$ ) to get a current of  $100\ \mu\text{A}$ . Simulate  $S_{I_D}$  the noise spectral density of drain current from 100 Hz to 100 MHz.

Double the length and resize  $W$  to get  $100\ \mu\text{A}$ , and simulate  $S_{I_D}$ . Repeat until  $L = 5.76\ \mu\text{m}$ . Overlay the spectral density plots (log y axis) and identify the  $1/f$  noise corners. Plot the  $1/f$  noise corners vs.  $L$ . Briefly explain the results.