EE539: Analog Integrated Circuit Design; HW2

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1. Make an opamp macromodel using controlled sources and passive components. It should model a linear transfer function $H(s) = \frac{1}{(1/A_o+s/\omega_u)(1+s/p_2)}$ with $Z_{in} = \infty$ and $Z_{out} = 0$. It should also model saturation at $\pm V_{max}$ volts. Show the schematic of the model and the component values in terms of the model parameters A_o, ω_u, p_2, and V_{max}.

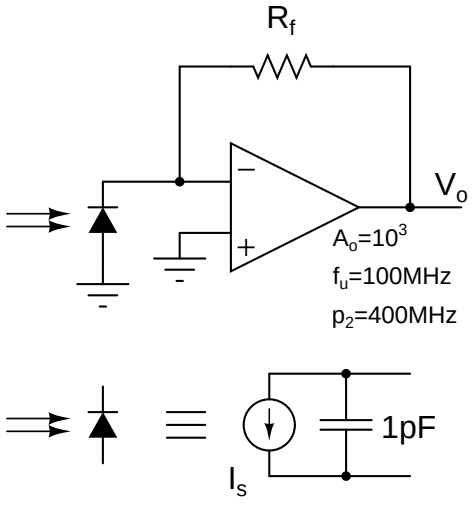

Figure 1: Problem 2

2. Fig. 1 shows a transimpedance amplifier driven by a photodiode. The photodiode can be modelled as a current source in parallel with a capacitor. The opamp has $A_o = 10^3$, $\omega_u/2\pi = 100\,\text{MHz}$ and $p_2/2\pi = 400\,\text{MHz}$. What is the largest transimpedance R_f you can have without peaking in the frequency response V_o/I_s? Show the ac magnitude response and the transient response to a current step of $1/R_f$ Amperes with a 100 ps risetime? Use the model in the previous problem with $V_{max} = 2\,\text{V}$.

   You are asked to increase the transimpedance by a factor of 10 using the same opamp. What happens to the ac and transient responses if you increase R_f by $10\times$? How can you modify the circuit to get $10\times$ transimpedance without introducing peaking in the frequency response? What is the largest bandwidth you can obtain under the above condition? Explain clearly with a schematic and simulation results. (For analytical calculations of maximally flat magnitude response, it'll be simpler to use an ideal integrator model for the opamp, and then adjust the values to account for the second pole).

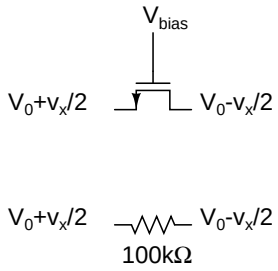

Figure 2: Problem 3

3. (For this problem, The minimum usable dimension is $0.5\,\mu$m.) A MOSFET is used as a $100\,\text{k}\Omega$ resistor (Fig. 2) $V_0 = 0.5\,V$ and v_x is restricted to 0.3 V. The difference in the current flowing through the MOS resistor and that in an ideal linear resistor must be at most 5% of the latter. Calculate the gate bias V_{bias} and the dimensions of the transistor. If a linear resistive material with a sheet resistance of $8\,\Omega$/sq. is available, what would be its dimensions? What is the motivation for using a transistor instead of a resistive material?

4. Design a 3 pF capacitor using A square nMOS device (drain/source shorted). Plot its capacitance as a

function of voltage (0 to 1.8 V). What is the usable voltage range of this capacitor?

Repeat the above for a square pMOS device.

A square Metal1-Metal2 structure.

A square sandwiched structure with poly, M2, M4 tied together and M1, M3, M5 tied together.

For the last two structures, determine the bottom plate parasitic capacitance.

Don't submit the following problems, just try them out. The following are to be simulated. Repeat for pMOS and nMOS.

1. Plot I_D vs. V_{DS} (0 to 1.8 V) for V_{GS} from 0 to 1.5 V in steps of 0.25 V and $V_{BS} = 0$ V. Overlay the plots for $W/L = 5\,\mu\text{m}/0.5\,\mu\text{m}$ and $W/L = 25\,\mu\text{m}/2.5\,\mu\text{m}$. Comment on the results.

2. Plot I_D vs. V_{DS} (0 to 1.8 V) for V_{BS} from -1 V to 0 V in steps of 0.25 V and $V_{GS} = 1.5$ V. Overlay the plots for $W/L = 5\,\mu\text{m}/0.5\,\mu\text{m}$ and $W/L = 25\,\mu\text{m}/2.5\,\mu\text{m}$. Comment on the results.

3. Plot (log-log) I_D vs. V_{GS} (18 mV to 1.8 V) for $V_{DS} = 1$ V and $V_{BS} = 0$ V. Overlay the plots for $W/L = 5\,\mu\text{m}/0.5\,\mu\text{m}$ and $W/L = 25\,\mu\text{m}/2.5\,\mu\text{m}$ and temperatures of $\{0, 27, 100\}^\circ$C. Comment on the results. Calculate the subthreshold slope η.

4. Plot (log-log) I_D vs. V_{BS} (-1.5 V to -15 mV) for $V_{DS} = 1$ V and $V_{GS} = 1$ V. Overlay the plots for $W/L = 5\,\mu\text{m}/0.5\,\mu\text{m}$ and $W/L = 25\,\mu\text{m}/2.5\,\mu\text{m}$ and temperatures of $\{0, 27, 100\}^\circ$C. Comment on the results.