EE539: Analog Integrated Circuit Design; HW7

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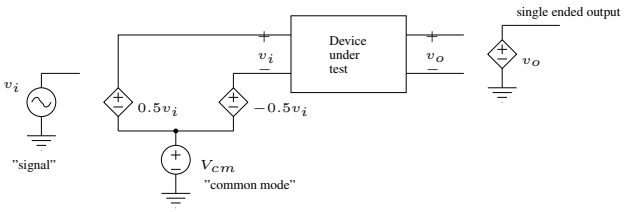

Figure 1: Test bench for differential circuits

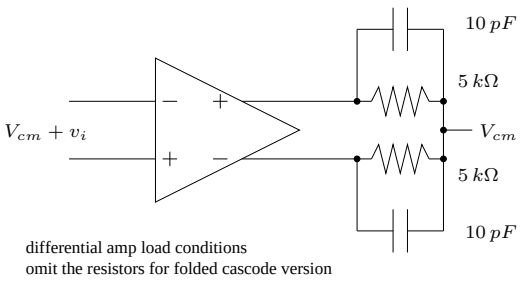

Figure 2: Differential opamp

$0.18\,\mu$m technology parameters: $V_{Tn} = 0.5\,$V; $V_{Tp} = 0.5\,$V; $K_n = 300\ \mu$A$/V^2$; $K_p = 75\ \mu$A$/V^2$; $A_{VT} = 3.5\,mV\,\mu$m; $A_\beta = 1\%\,\mu$m; $V_{dd} = 1.8\,$V; $L_{min} = 0.18\ \mu$m, $W_{min} = 0.24\ \mu$m; Ignore body effect unless mentioned otherwise. Ignore 1/f noise unless mentioned otherwise.

For testing differential circuits, the circuit in Fig. 1 can be used to preserve symmetry and avoid errors (such as not driving the inputs symmetrically). v_i can be the desired signal (ac, dc, or transient). When v_i is the input source for noise analysis, the input referred noise refers to the differential input.

A similar test bench can be created for common mode input/outputs by appropriately changing the controlled sources.

For differential opamps in this assignment, you should not have redesign anything. You only need to turn the opamps already designed in previous assignments to fully differential versions and add common mode feedback circuitry. Use $V_{cm} = 0.9\,$V Report the following for all opamp designs and show simulation results where appropriate.

- Input common mode range
- Output voltage range
- Open loop and closed loop frequency responses
- An estimate of poles and zeros of the circuit (open and closed loop)
- DC sweep of the buffer with input varying from 0 to Vdd
- Transient response of the unity gain buffer with a +0.1 V step and a -0.1 V step (use 1 ns rise/fall times). Report the slew rate and compare it with the theoretical value.
- Input referred noise spectral density-identify 1/f noise corner if applicable.
- Input referred rms offset voltage due to random mismatch. Ignore current factor mismatch.
- Power consumption
- Show a schematic with all sizes and operating points (g_m, g_{ds}, V_{GS}-V_T, I_D) of all transistors and the node voltages.

Do not use an ideal current source in the tail. You can use one ideal reference current source of 1/10$^{\text{th}}$ the tail current for bias generation.

1. Turn the folded cascode opamp designed in assignment 6 to a fully differential version. Use the cir-

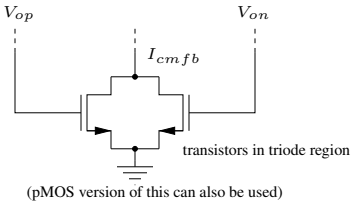

Figure 3: Common mode feedback structure for folded cascode opamp

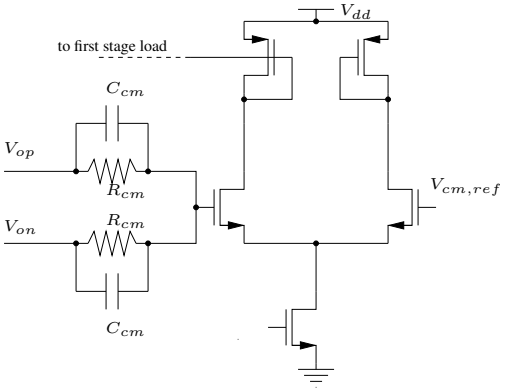

Figure 4: Common mode feedback structure for two stage opamp

cuit in Fig. 3 for common mode feedback. Size the CMFB transistors to have 50 mV across them in quiescent condition. Report the following and show simulation results where appropriate.

(a) Input common mode range

(b) Output voltage range

(c) Open loop frequency response

(d) An estimate of poles and zeros of the circuit

(e) Input(differential) referred noise spectral density-identify 1/f noise corner if applicable.

(f) Power consumption

(g) Show a schematic with all sizes and operating points (g_m, g_{ds}, V_{GS}-V_T, I_D) of all transistors and the node voltages.

2. Turn the two stage opamp in P3 of the previous assignment above into a fully differential version. Use the circuit in Fig. 4 for common mode feedback. Report the same quantities as above.

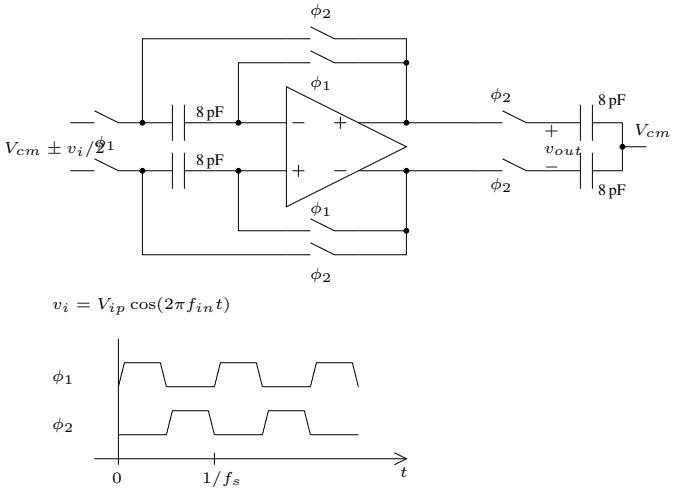

Figure 5: Sample and hold circuit

3. Use the opamps in P2 and P3 (fully differential opamps designed earlier) in the sample hold circuit in Fig. 5. Use ideal switches with 1 kΩ on resistance. Use $f_s = 4$ MHz and $f_{in} = \{1/4, 9/4\}$ MHz (sinusoidal input with 1.6 Vppd[1] amplitude) and plot the output waveforms.

4. Simulate the response of the circuit in Fig. 6 to a differential step of 1 V and plot the output. Also plot the output for a 0.5 V common mode step. Use the two stage fully differential opamp designed above.

Don't submit the following problems, just try them out.

1. **Bandgap reference**: Bias a 1x sized diode connected PNP[2] at 10 μA as shown in Fig. 7(a) and sweep the temperature from 0 to 100°C. Determine dV_{BE}/dT at 27°C.

   Design the bandgap shown in Fig. 7(c). Choose R_1 for a quiescent current of 10 μA and R_2 to get zero temperature coefficient at V_{bg}. Choose $R_3 = R_2$. What is the role of R_3? Simulate the bandgap reference with the model of a single stage opamp designed in HW5 (Fig. 7(b)-model the gm, and the pole zero doublet). Choose C_c so that the phase margin is 60°. Test the transient response by applying a 1 uA pulse to the output of the opamp. Simulate over tem-

[1] Vppd: volts, peak-peak differential

[2] Use the model `ideal_pnp` in `ideal_diode.lib`

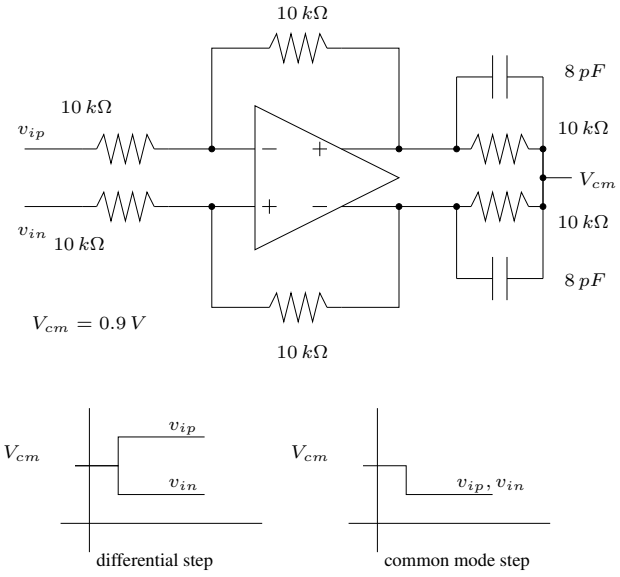

Figure 6: Inverting amplifier

perature and plot V_{bg}. Adjust the values of R_1, R_2, R_3 $(= R_2)$ to get zero TC at 27°C.

Modify the circuit as in Fig. 7(d). How should V_x, V_y, and V_{bg} change? What is the purpose of this modification? Resimulate with the opamp model as before and test the temperature sensitivity, transient response and the loop gain.

Substitute the opamp designed in HW5 and simulate the temperature sensitivity and loop gain.

2. **Constant g_m biasing**: Simulate the transconductance and the open loop frequency response (V_o/V_{id}) of the telescopic cascode opamp designed in HW6 over 0-100°C range. Design a constant g_m biasing circuit so that the current at room temperature is the same as the fixed bias used previously. Resimulate the transconductance and the open loop frequency response of the opamp. Comment on the results.

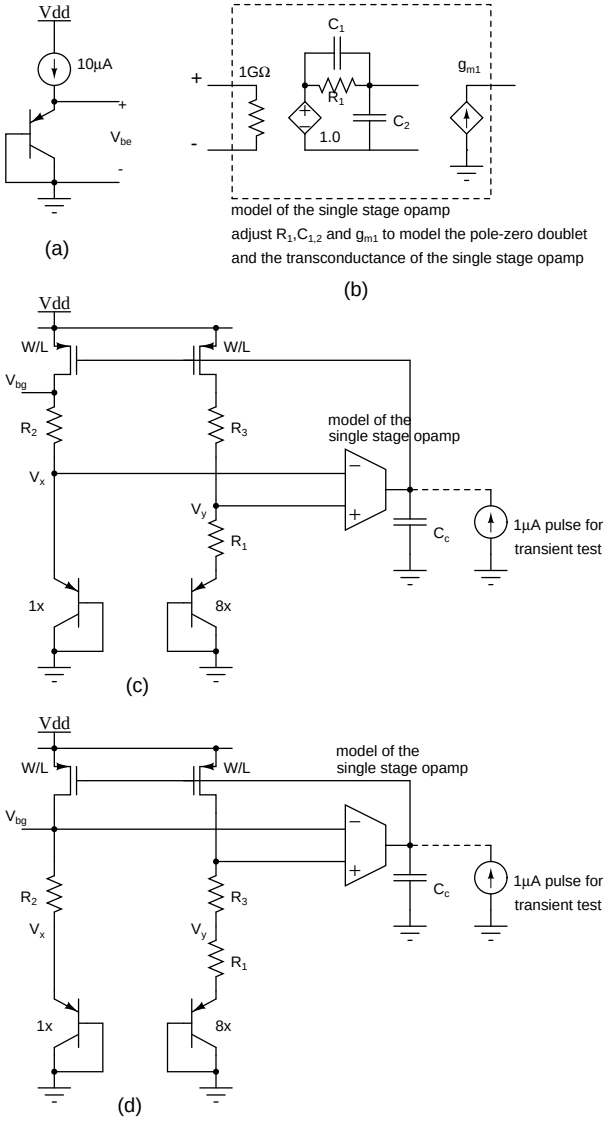

Figure 7: Bandgap reference