EE539: Analog Integrated Circuit Design; HW6

Nagendra Krishnapura (nagendra@iitm.ac.in)

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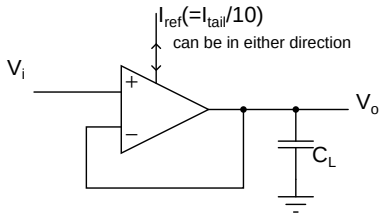

Figure 1: Unity gain buffer with an opamp

0.18 μm technology parameters: $V_{Tn} = 0.5$ V; $V_{Tp} = 0.5$ V; $K_n = 300\ \mu\text{A}/V^2$; $K_p = 75\ \mu\text{A}/V^2$; $A_{VT} = 3.5\,mV\,\mu$m; $A_\beta = 1\%\,\mu$m; $V_{dd} = 1.8$ V; $L_{min} = 0.18\ \mu$m, $W_{min} = 0.24\ \mu$m; Ignore body effect unless mentioned otherwise. Ignore 1/f noise unless mentioned otherwise. Report the following for all opamp designs and show simulation results where appropriate.

- Input common mode range
- Output voltage range
- Open loop and closed loop frequency responses
- An estimate of poles and zeros of the circuit (open and closed loop)
- DC sweep of the buffer with input varying from 0 to Vdd
- Transient response of the unity gain buffer with a +0.1 V step and a -0.1 V step (use 1 ns rise/fall times). Report the slew rate and compare it with the theoretical value.
- Input referred noise spectral density-identify 1/f noise corner if applicable.
- Input referred rms offset voltage due to random mismatch. Ignore current factor mismatch.
- Power consumption
- Show a schematic with all sizes and operating points (g_m, g_{ds}, V_{GS}-V_T, I_D) of all transistors and the node voltages.

Do not use an ideal current source in the tail. You can use one ideal reference current source of 1/10$^{\text{th}}$ the tail current for bias generation (Fig. 1).

1. Turn the single stage opamp designed in the previous assignment into a telescopic cascode opamp[1]. Use cascode devices of the same size as the respective devices. Design the biasing circuit for the cascode devices to maximize the swing.
2. Turn the single stage opamp designed in the previous assignment into a folded cascode opamp[1]. Ensure that the slew rate limitations due to the first and the second stage are identical. Design the biasing circuit for the cascode devices to maximize the swing.
3. Design a two stage single ended opamp (Fig. 2) that has a dc gain of at least 1000, and a unity gain frequency of 100 MHz with a load of 10 pF and 5 kΩ in parallel. Design the second stage common source amplifier to have a sufficiently high dc gain while driving the desired load resistance and a sufficiently high second pole while driving the desired load capacitance. Use a scaled version[2] of your single stage opamp design from the previous assignment for the input stage. Use a suitable compensation capacitor (Fig. 2). All parasitic poles and zeros should be at at least twice the unity gain frequency. Ensure that

[1] Do not redesign the circuit except for the addition of cascode devices and suitable bias circuitry

[2] You should not have to redesign this stage

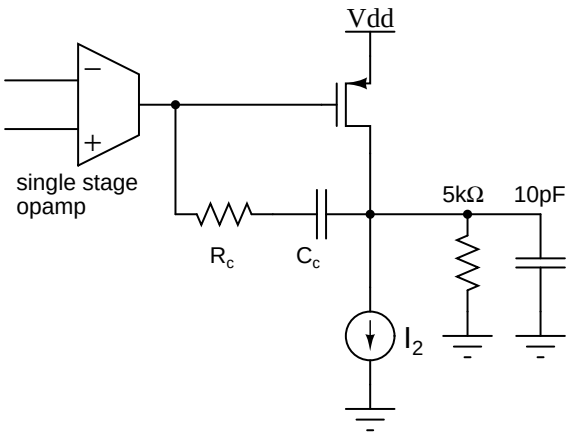

Figure 2: Two stage opamp

there is no systematic offset because of the second stage bias. Add a zero canceling resistor.