EE539: Analog Integrated Circuit Design; HW5

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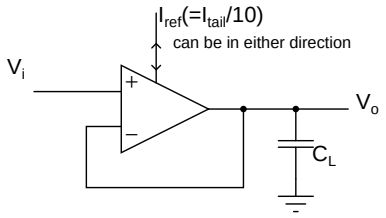

Figure 1: Unity gain buffer with an opamp

0.18 μm technology parameters: $V_{Tn} = 0.5$ V; $V_{Tp} = 0.5$ V; $K_n = 300\ \mu\text{A}/V^2$; $K_p = 75\ \mu\text{A}/V^2$; $A_{VT} = 3.5\,mV\ \mu$m; $A_\beta = 1\%\,\mu$m; $V_{dd} = 1.8$ V; $L_{min} = 0.18\ \mu$m, $W_{min} = 0.24\ \mu$m; Ignore body effect unless mentioned otherwise.

1. Design a single stage single ended opamp with a dc gain of 40 using an nMOS differential pair. The application is a unity gain buffer with 0.5 Vpp (± 0.25 V around the common mode) swing. The unity gain buffer should have a 3 dB bandwidth of 100 MHz, with $C_L = 10$ pF. All parasitic poles and zeros should be at at least twice the unity gain frequency. Report the following and show simulation results where appropriate.
   (a) Input common mode range
   (b) Output voltage range
   (c) Open loop and closed loop frequency responses
   (d) An estimate of poles and zeros of the circuit (open and closed loop)
   (e) DC sweep of the buffer with input varying from 0 to Vdd
   (f) Transient response of the unity gain buffer with a +0.1 V step and a -0.1 V step (use 0.1 ns rise/fall times). Report the slew rate and compare it with the theoretical value. (If you don't see slewing, increase the step amplitude until you do)
   (g) Input referred noise spectral density-identify 1/f noise corner if applicable.
   (h) Power consumption
   (i) Show a schematic with all sizes and operating points (g_m, g_{ds}, V_{GS}-V_T, I_D) of all transistors and the node voltages.

   Do not use an ideal current source in the tail. You can use one ideal reference current source of 1/10$^{\text{th}}$ the tail current for bias generation (Fig. 1).

   Try to determine as many parameters as possible from the specifications and choose sensible starting points for the others. Try to adjust the channel lengths so that g_{ds} contributions from nMOS and pMOS sides are equal (This is not the only possible choice. Other choices may be preferable to optimize other figures of merit-e.g. noise. This is a suggested starting point for simplicity). Choose an appropriate common mode voltage.

   Maximize the output voltage swing and reduce the power consumption during the design.

2. Fig. 2(a) shows a macromodel of an opamp with two non dominant poles. Determine the transfer function of the opamp, its dc gain, poles and zeros, and the unity gain frequency. Determine the values for $A_{dc} = 500$, $\omega_u = 100$ MHz, $p_2 = 200$ MHz, $p_3 = 400\,MHz$. Simulate the unit step response of the circuit. Use a 10ps risetime for the input step.

   Plot the step response in the following cases (In each case all other parameters have their nominal values). a) $\omega_u = \{100, 200\}$ MHz, $p_2 =$

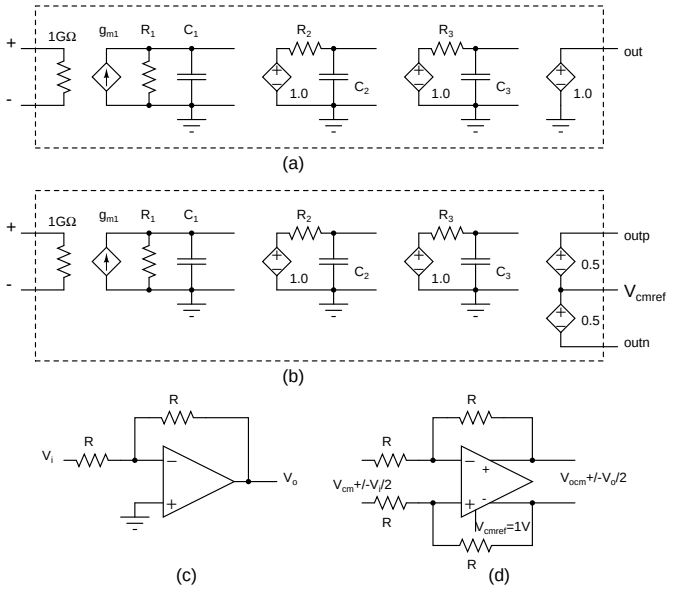

Figure 2: Problem 3

$3\omega_u$, $p_3 = 4\omega_u$. b) $\omega_u = \{100, 200\}$ MHz c) $p_2 = p_3 = \{150, 200, 300, 1000\}$ MHz, d) $p_2 = \{100, 200, 300\}$ MHz, $p_3 = \infty$, e) $A_{dc} = \{20, 50, 100, 500\}$. Explain the results.

Fig. 2(c) shows a macromodel of a fully differential opamp with two non dominant poles. V_{cmref} controls the output common mode. Determine the values for $A_{dc} = 500$, $\omega_u = 100$ MHz, $p_2 = 300$ MHz, $p_3 = 400\,MHz$. Simulate the response of the amplifier in Fig. 2(d) to a differential unit step. Use $V_{cmref} = 1\,V$ and $V_{cm} = 0.5\,V$. Plot V_{op}, V_{on} and verify that they have expected values.

Plot the differential and common mode step response[1] in the following cases (In each case all other parameters have their nominal values). a) $\omega_u = \{100, 200\}$ MHz, $p_2 = 3\omega_u$, $p_3 = 4\omega_u$. b) $\omega_u = \{100, 200\}$ MHz c) $p_2 = p_3 = \{150, 200, 300, 1000\}$ MHz, d) $p_2 = \{100, 200, 300\}$ MHz, $p_3 = \infty$, e) $A_{dc} = \{20, 50, 100, 500\}$. Explain the results.

3. $g_{m1} = 20\mu$S, $g_{ds1} = 1\mu$S, $g_{m2} = 80\mu$S, $g_{ds2} = 1\mu$S, $G_L = 1\mu$S, $C_{gs_1} = 10$ fF, $C_{gs_2} = 40$ fF,

[1]While measuring the differential step response, the common mode voltage is held constant; While measuring the common mode step response, the differential voltage is zero

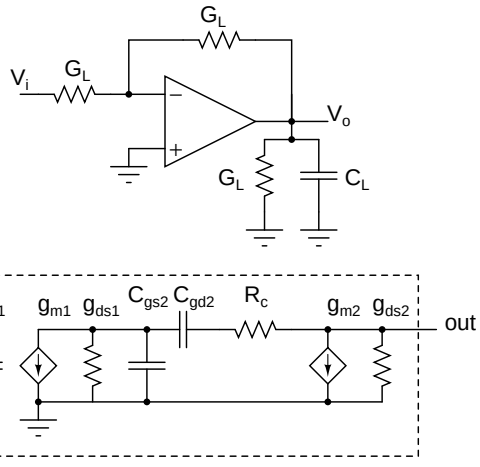

Figure 3: Problem 3

$C_{gd_2} = 250$ fF, $C_L = 1$ pF, $R_c = 12.5\,\text{k}\Omega$. Simulate the circuit for the following cases: Vary each of C_{gs_1}, C_{gs_2}, C_{gd_2}, C_L, G_L, R_c, from $0.1\times$ their nominal value to $10\times$ their nominal value, with 2 steps per decade. In each case keep all the other components at their nominal values.

Plot the unit step response and loop gain (overlaid on the same plot for each case). Comment on the results.