# EE539: Analog Integrated Circuit Design; HW2

Nagendra Krishnapura (nagendra@iitm.ac.in)

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$0.18\,\mu$m technology parameters: $V_{Tn} = 0.5\,$V; $V_{Tp} = 0.5\,$V; $K_n = 300\ \mu\text{A}/V^2$; $K_p = 75\ \mu\text{A}/V^2$; $A_{VT} = 3.5\,mV\,\mu$m; $A_\beta = 1\%\,\mu$m; $V_{dd} = 1.8\,$V; $L_{min} = 0.18\ \mu$m, $W_{min} = 0.24\ \mu$m; Ignore body effect unless mentioned otherwise.

1. Plot the $f_T$ of an nMOS device (biased with $V_{GS} = 1\,$V) versus $L$ with $W/L$ doubling at each step from $4\,\mu\text{m}/0.2\,\mu\text{m}$ to $128\,\mu\text{m}/6.4\,\mu\text{m}$. Comment on the results.

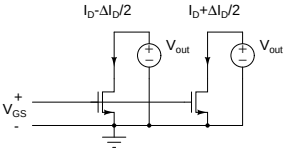


Figure 1:

2. Two transistors carrying a current $I_D$ are required to have a current mismatch $\leq \sigma_{I_D}$ and operate in saturation with an output voltage $V_{out}$ (Fig. 1). Compute the transistor dimensions and its $f_T$ in terms of the mismatch constants $A_{VT}$ and $A_\beta$, $I_D$, $\sigma_{I_D}$ and $V_{out}$. Comment on tradeoffs between speed, voltage, and precision.

3. Bias a pMOS transistor with $V_{GS} = V_{DS} = 1\,V$ and determine $W$ (with $L = 0.2\,\mu$m) to get a current of $100\,\mu$A. Simulate $S_{I_D}$ the noise spectral density of drain current from 100 Hz to 100 MHz. Double the length and resize $W$ to get $100\,\mu$A, and simulate $S_{I_D}$. Repeat until $L = 6.4\,\mu$m. Overlay the spectral density plots (log y axis) and identify the $1/f$ noise corners. Plot the $1/f$ noise corners vs. $L$. Briefly explain the results.

4. Repeat the previous simulations for nMOS. How do the noise of nMOS and pMOS transistors compare for the same channel length?

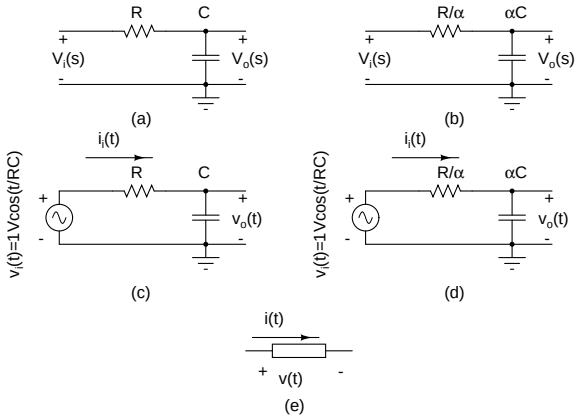


Figure 2:

5. For the circuits in Fig. 2(a) and Fig. 2(b), evaluate the transfer function $H(s) = V_o(s)/V_i(s)$ and the output rms noise voltage.

6. In the circuits in Fig. 2(c) and Fig. 2(d), evaluate the current $i_i(t)$ through the input voltage source. Evaluate the average power dissipated in the voltage source and the resistor, and the output rms signal voltage. Compare the signal

to noise ratio $(S/N)$ and the power dissipation of the two circuits.

7. Evaluate analytically the output signal to noise ratio $(S/N)$ for an input peak voltage $V_p$, the power dissipation $P$ in the resistor, and the bandwidth $f_b$ (in Hz) of the circuit in Fig. 2(c). Express the power dissipation in terms of $S/N$ and $f_b$. What tradeoff does this expression represent?

Don't submit the following problems, just try them out.

1. Plot $g_m$, $g_{ds}$, $g_{mbs}$, $g_m/g_{ds}$, $f_T$, $V_{GS}$, and $V_{DS,SAT}$[1] as a function of $I_D$ (from $2\,\mu$A to $200\,\mu$A) for a diode connected nMOS transistor for two cases: $W/L = 5\,\mu\text{m}/0.5\,\mu\text{m}$ and $W/L = 25\,\mu\text{m}/2.5\,\mu\text{m}$. In each case, overlay the plots for 0°C and 100°C.

2. Repeat the previous problem for pMOS.

3. Textbook problem 2.12 (Textbook Fig. 2.49)

[1] $g_m$, $g_{ds}$, $g_{mbs}$, $V_{GS}$, and $V_{DS,SAT}$ will be reported by the simulator at the dc operating point. Calculate $f_T$