EE539: Analog Integrated Circuit Design; HW1

Nagendra Krishnapura (nagendra@iitm.ac.in)

due on 17 Jan. 2007

Submit all solutions by email as a single pdf file; Present the solutions in the same order as the problems below.

0.18 μm technology parameters: $V_{Tn} = 0.5$ V; $V_{Tp} = 0.5$ V; $K_n = 300\ \mu\text{A}/V^2$; $K_p = 75\ \mu\text{A}/V^2$; $A_{VT} = 3.5\,mV\ \mu$m; $A_\beta = 1\%\,\mu$m; $V_{dd} = 1.8$ V; $L_{min} = 0.18\ \mu$m, $W_{min} = 0.24\ \mu$m; Ignore body effect unless mentioned otherwise.

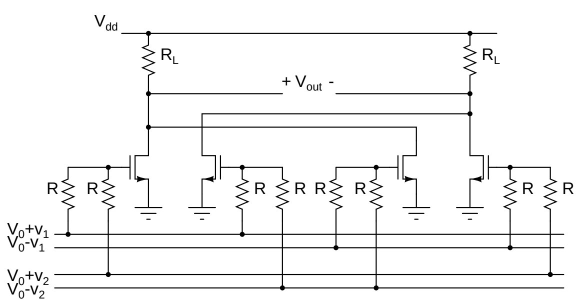

Figure 1: Problem 1

1. Calculate V_{out} in Fig. 1. What is the function of the circuit? (Assume that all transistors are in the saturation region)

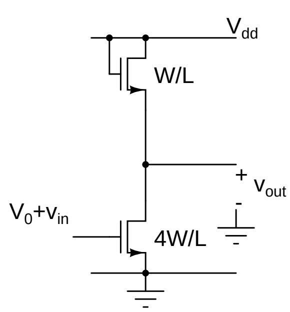

Figure 2: Problem 2

2. Calculate V_{out} in Fig. 2. Comment. (Assume that all transistors are in the saturation region)

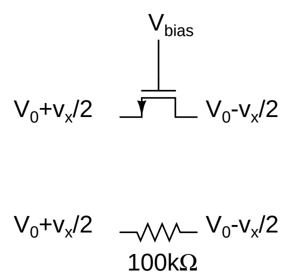

Figure 3: Problem 3

3. (For this problem, The minimum usable dimension is $0.25\,\mu$m.) A MOSFET is used as a $200\,\text{k}\Omega$ resistor (Fig. 3) $V_0 = 0.5\,V$ and v_x is restricted to 0.2 V. The nonlinear part of the current in the resistor should be at most 5%. Calculate the gate bias V_{bias} and the dimensions of the transistor. If a linear resistive material with a sheet resistance of 8 Ω/sq. is available, what would be its dimensions? What is the motivation for using a transistor instead of a resistive material?

4. Simulate and plot (overlaid) the magnitude and phase response of the circuit shown in Fig. 4 using the four resistor models shown. $R = 10\,\text{k}\Omega$, $C = 1.5$ pF. Comment on the results.

5. Design a 0.5 pF capacitor using A square nMOS device (drain/source shorted). Plot its capacitance as a function of voltage (0 to 1.8 V). What

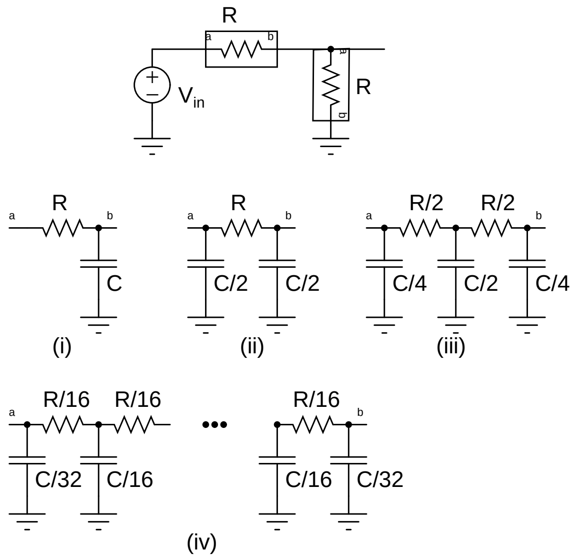

Figure 4: Problem 4

is the usable voltage range of this capacitor?

Repeat the above for a square pMOS device.

A square Metal1-Metal2 structure.

A square sandwiched structure with poly, M2, M4 tied together and M1, M3, M5 tied together.

For the last two structures, determine the bottom plate parasitic capacitance.

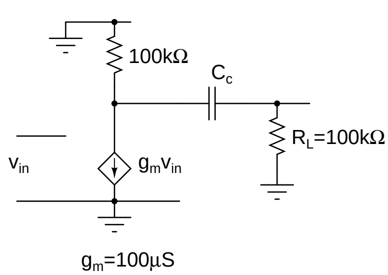

Figure 5: Problem 5

6. Determine the value of the ac coupling capacitor C_c in Fig. 5 so that it and the load capacitor form a highpass filter with a cutoff frequency of $10/\pi$ MHz.

   Design the desired C_c using the last two options in the previous problem. Simulate the circuit including the parasitics with a) an ideal capacitor, b) M1-M2 capacitor with both orientations, and c) poly-M1-M2-M3-M4-M5 sandwich with both orientations. Overlay the magnitude response plots. Comment on the results.

Don't submit the following problems, just try them out.

1. Textbook problem 2.6 (Textbook Figure 2.43). I_x and g_m of M_1.

The following are to be simulated. Repeat for pMOS and nMOS.

1. Plot I_D vs. V_{DS} (0 to 1.8 V) for V_{GS} from 0 to 1.5 V in steps of 0.25 V and $V_{BS} = 0$ V. Overlay the plots for $W/L = 5\,\mu\text{m}/0.5\,\mu\text{m}$ and $W/L = 25\,\mu\text{m}/2.5\,\mu\text{m}$. Comment on the results.

2. Plot I_D vs. V_{DS} (0 to 1.8 V) for V_{BS} from -1 V to 0 V in steps of 0.25 V and $V_{GS} = 1.5$ V. Overlay the plots for $W/L = 5\,\mu\text{m}/0.5\,\mu\text{m}$ and $W/L = 25\,\mu\text{m}/2.5\,\mu\text{m}$. Comment on the results.

3. Plot (log-log) I_D vs. V_{GS} (18 mV to 1.8 V) for $V_{DS} = 1$ V and $V_{BS} = 0$ V. Overlay the plots for $W/L = 5\,\mu\text{m}/0.5\,\mu\text{m}$ and $W/L = 25\,\mu\text{m}/2.5\,\mu\text{m}$ and temperatures of $\{0, 27, 100\}$°C. Comment on the results. Calculate the subthreshold slope η.

4. Plot (log-log) I_D vs. V_{BS} (-1.5 V to -15 mV) for $V_{DS} = 1$ V and $V_{GS} = 1$ V. Overlay the plots for $W/L = 5\,\mu\text{m}/0.5\,\mu\text{m}$ and $W/L = 25\,\mu\text{m}/2.5\,\mu\text{m}$ and temperatures of $\{0, 27, 100\}$°C. Comment on the results.