Audio at Low and High Power

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***Abstract*— An overview is presented of recent developments in the analog boundaries of the audio chain. The main focus is on class-D amplifiers that are by now almost standard in consumer applications and emerging in automotive and mobile applications as well. Further, an overview of the state-of-the-art in A/D and D/A conversion is given.**

I. INTRODUCTION

The acquisition and reproduction of audio signals was among the first applications of electronic circuits. Nowadays, audio electronics are ubiquitous and can be found in television and hifi-stereo sets, car audio systems and more recently in cellular phones and many other portable applications. The vast majority of these electronics is in the form of integrated circuits. A generic audio chain is shown in figure 1. Nowadays, almost all audio sources are digital with the exception of microphone and line inputs. In case of an analog input it is desirable to convert to the digital domain as soon as possible using an analog-to-digital converter (ADC). A programmable gain amplifier (PGA) adjusts the input signal level to maximize the dynamic range of the ADC.

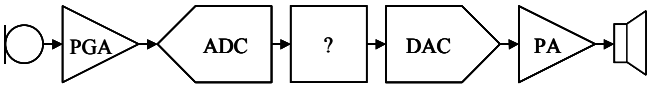

Figure 1. Generic audio processing chain.

At the end of the chain the signal is converted back to analog by a digital-to-analog converter (DAC) and amplified by a power amplifier (PA) before it is delivered to the load. This load can be a loudspeaker, a headphone or a line load. The digital connection between the analog boundaries can be anything ranging from digital signal processing, wired and/or wireless communication links (telephone) to storage and playback systems (CD-player). A system containing a plurality of all these elements in the audio chain is called an *audio codec*. However partitioning of the audio chain is possible in many different ways. The PA is often realized in a dedicated technology allowing for higher voltages and more power. Also ADCs and DACs are available as stand alone parts. The emergence of battery fed applications such as cellular phones and MP3 players has driven the need for reduced power consumption. The current trend is to make the audio chain configurable so that power can be exchanged for performance. On the PA side a gradual but definite shift has taken place from linear class-AB to high efficiency class-D amplifiers.

II. ANALOG TO DIGITAL CONVERSION

The use of ΣΔ modulators in audio ADCs and DACs has already been popular since the 1980's. This is due to the fact that the high-resolution, high-linearity and low-bandwidth audio requirements naturally fit to the characteristics of a one-bit ΣΔ modulator. Today, the ΣΔ modulator has become a versatile solution for many different standards, ranging from sensor applications, audio, AM/FM radio, cellular to connectivity with signal bandwidths in the range from a few Hertz to several tens of MegaHertz. Numerous techniques such as higher-order filters, multi-bit quantizers, cascaded (or MASH) topologies, continuous-time and switched-capacitor filter implementations, data-weighted averaging algorithms, etc. have been pushing the ΣΔ modulator performance to new state-of-the-art data points in terms of bandwidth, resolution, power and figure-of-merit. Many of these techniques also find their entry in audio ΣΔ modulators, as modern technologies put new challenges and constraints on the design of ΣΔ modulators and require different solutions than the traditional one-bit ΣΔ modulator architecture.

A. Switched-capacitor versus switched-current design

The main requirements for audio ΣΔ modulators are: low-voltage, low power, medium to high accuracy and low-cost. High-end audio ADCs have distortion figures better than 95dB and a dynamic range of 100dB. The decreasing feature size of newer technologies, accompanied by a lower supply voltage imposes new challenges for ΣΔ designs. Traditionally, switched-capacitor (SC) implementations of audio ΣΔ modulators are favored over switched-current continuous-time (CT) designs. Switched-capacitor ΣΔ modulators are known for their clock jitter tolerance, precise filter coefficients (defined by capacitor ratios), and high linearity. Moreover, as flicker noise is one of the dominant noise sources in audio ΣΔ modulators, the employment of chopper stabilization techniques is relatively simple in SC designs [1]. Another practical aspect of SC ΣΔ modulators is that they can be scaled

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with the sampling frequency. A SC ΣΔ modulator can be utilized at different sampling rates without the need for changing the filter coefficients. This way, the bandwidth of the modulator or the audio data rate can be easily scaled. Continuous-time ΣΔ modulators are less clock jitter tolerant, are not scaled easily with the sampling frequency, and compared to SC designs, incorporation of choppers in CT implementations is less common practice.

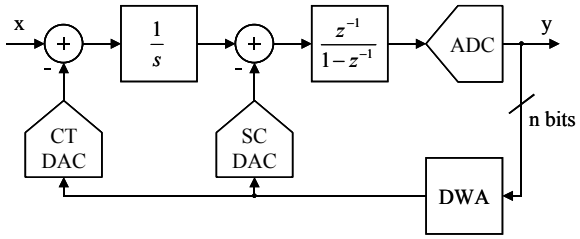

Figure 2. Combined CT/SC ΣΔ architecture [1]

Continuous-time ΣΔ modulators offer different advantages that have become more and more attractive recently. A CT ΣΔ modulator does not need sampling switches at the input. As the supply voltage lowers for each new technology node, it has become increasingly more difficult to design a high linearity switch. Techniques like voltage boosting and bootstrapping increase the switch performance, but come with a power and area penalty. A CT ΣΔ modulator does not suffer from the switch problem. Another implication of a lowering supply voltage is the reduction of the maximum input signal swing. The lower the input signal amplitude becomes, the lower the circuit noise has to be designed in order to achieve the required resolution. This results in higher power consumption. Utilizing the maximum possible input signal amplitude is therefore from utmost importance, but is difficult to interface to a SC ΣΔ modulator because of the earlier mentioned sampling switch non-linearity. This is one of the main reasons why several recently published audio ΣΔ modulators utilize CT input stages [1,2] as shown in figure 2. Also, CT ΣΔ modulators have been shown to be very power efficient, which is attractive for battery-operated products like portable MP3 players, mobile phones, etc. As the input stage of a CT ΣΔ modulator is resistive, it does not introduce EMI radiation to the input pins of the ADC, which is an issue with SC modulators as a result of clock feed-through of the input sampling stage [2]. Furthermore, a continuous-time ΣΔ modulator has inherent anti-alias suppression, which results in better noise immunity.

B. Audio ΣΔ modulator architectures

To achieve the low quantization noise levels that are needed for high-resolution audio ΣΔ modulators, different architectures can be used, ranging from higher-order one-bit topologies to multi-bit modulators with low-order loopfilters, all with their specific pros and cons. Single-bit ΣΔ modulators have the advantage of superior linearity over multi-bit modulators due to the employment of an inherently linear one-bit DAC. However, one-bit converters suffer from idle in-band tones and require high slew rate, fast settling opamps due to the large error step size [3]. Multi-bit ΣΔ modulators can achieve similar quantization noise suppression as one-bit converters at a lower sampling frequency and/or filter order [1]. Moreover, multi-bit ΣΔ modulators suffer much less from idle channel tones and have more relaxed opamp requirements due to the smaller error step size. On the other hand, a multi-bit DAC introduces mismatch induced non-linearity in the ΣΔ modulator that puts a limit to the maximum achievable harmonic distortion. Mismatch-shaping algorithms like data-weighted averaging (DWA) with first-order [4,1,2] and second-order [5] spectral shaping of static DAC errors overcome the harmonic distortion limitation and enable the use of multi-bit DACs in high-performance low-distortion audio converters (Figure 2).

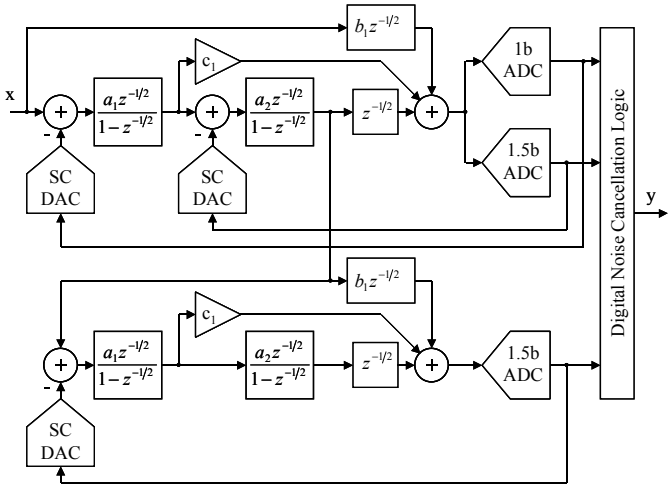

Figure 3. MASH ΣΔ architecture [6]

Employing a cascaded or MASH (multi-stage noise shaping) ΣΔ modulator topology is a way to achieve high resolution at a much lower oversampling factor compared to single-loop converters. A MASH type ΣΔ modulator incorporates multiple cascaded ΣΔ modulators that process the quantization error of the previous stage. Figure 3 shows a 2-2 MASH ΣΔ architecture for an audio ADC [6]. The lower loop digitizes the quantization error of the upper loop. With digital noise cancellation logic, the quantization noise of the upper loop is highly suppressed. Besides quantization noise, idle tones are also suppressed by the noise cancellation logic. As a result, the architecture proposed in figure 3 combines the excellent linearity of a one-bit feedback DAC in the first ΣΔ loop without the idle tone problems of a single loop one-bit modulator.

III. CLASS-D POWER AMPLIFIERS

The most important feature of class-D amplifiers is high efficiency that typically is higher than 90% at full output power. This efficiency allows very high output power with modest heat sinking. Output powers well over 100W per channel are no exception [7,8]. Integrated class-D amplifiers typically have distortion better than 70dB and a dynamic range of 100dB.

A basic class-D amplifier is shown in figure 4. At the heart of a class-D amplifier are two low-ohmic switches that

alternately connect the output node to the positive or negative supply rail. Usually, some form of Pulse Width Modulation (PWM) is used to encode the audio signal. The audio signal is subsequently retrieved by means of an external LC lowpass filter connected between the class-D output stage and the load.

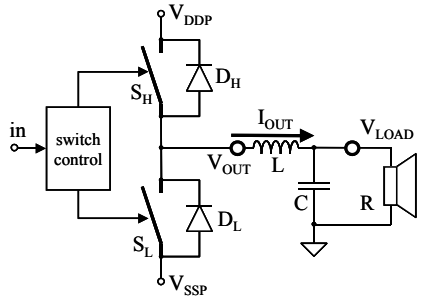

Figure 4. Basic class-D amplifier.

The simplest form of PWM is so-called natural sampling PWM or NPWM [9]. A NPWM signal can easily be constructed by comparing the audio signal to a triangular reference as shown in figure 5. The fundamental frequency of the triangular reference is usually much higher than the highest audio frequency, e.g. around 350kHz or 8*44.1kHz, and is called the carrier frequency.

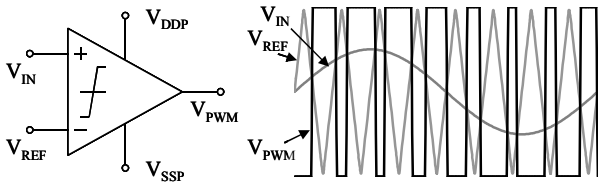

Figure 5. Natural sampling PWM.

The *modulation depth M* is defined between +1 and –1 and is related to the duty-cycle *D* of the PWM signal as:

$$M = 2 \cdot D - 1 \tag{1}$$

Although the generation of NPWM involves a highly nonlinear comparator the frequency spectrum of a NPWM does not contain harmonics of the input signal but only intermodulation products of the carrier and the input signal, i.e., NPWM is free from harmonic distortion. Assuming that the triangular reference has a sufficiently high frequency, the intermodulation products do not fold back to the audio frequency band and are filtered out by the LC lowpass filter. In a practical implementation it is not possible to reproduce the PWM pulses at the output with mathematical precision because the switching output stage introduces timing and amplitude errors that result in distortion.

A class-D output stage can be either single-ended (SE) or differential, yielding a so-called bridge-tied-load (BTL) configuration as shown in figure 6. In a BTL amplifier both sides of the loudspeaker load are driven in opposite (audio) phase. This enables operation from a single supply while doubling the voltage swing across the load, yielding four times more output power than a SE amplifier. Furthermore, the balanced operation cancels out even order distortion. On the downside, a BTL amplifier needs twice the number of power switches and inductors making it relatively expensive.

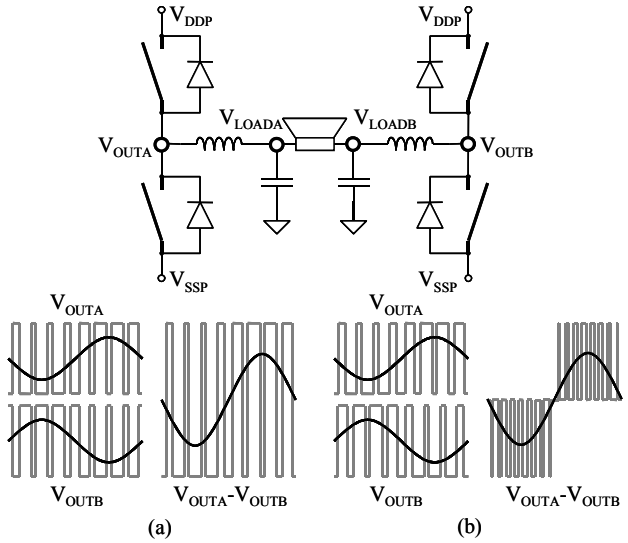

Figure 6. BTL configuration with (a) AD modulation (b) BD modulation.

In a BTL class-D amplifier the phase of the carriers of both bridge halves can be chosen independently. When the carriers are in opposite phase, as shown in figure 6(a), this is called AD-modulation. The main advantage of AD-modulation is that the output signal has zero common-mode since the bridge halves always switch simultaneously in opposite directions. Conversely, when the carriers are in-phase carriers, as shown in figure 6(b), this is called BD-modulation. Compared to AD-modulation, BD-modulation is much less sensitive to clock jitter. [10]. In practice both modulation types are being used.

IV. Class-D Amplifier Architecture

Many Class-D amplifier architectures exist. A coarse division can be made in *open loop* and *closed loop* architectures.

A. Open Loop Architectures

In open loop class-D amplifiers the PWM signal is generated in the digital domain and directly drives a class-D output stage. In this architecture the class-D output stage itself serves as DAC. Because the PWM signal is generated in the digital domain the effects of *sampling* and *quantization* have to be dealt with.

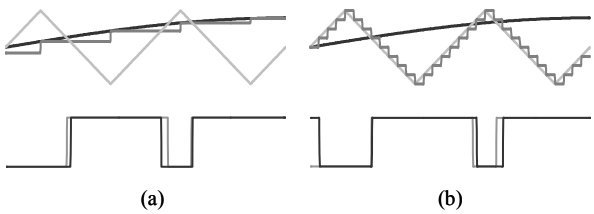

Figure 7. Digital PWM (a) sampling (b) quantization.

A sampled input signal intersects the reference triangle at different moment than the original modulating signal as

illustrated in figure 7(a). The resulting shift of the PWM signal edges cause distortion. In a digital PWM modulator the edges are synchronized to a high-frequency bit-clock, e.g. $256f_s$. Consequently, the pulse widths are quantized to a limited number of discrete values as illustrated in figure 7(b) causing quantization noise.

Sampling and quantization effects can be handled separately or integrally. In a separated approach as shown in figure 8(a) first the distortion caused by sampling is corrected by either approximating NPWM using linear or higher order interpolation [9] or applying pre-correction based on a digital PWM distortion model [11]. Secondly, the quantization noise is shaped out-of-band by a ΣΔ modulator before converting to digital PWM.

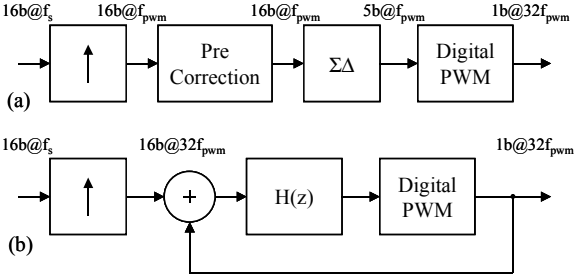

Figure 8. Digital PWM (a) precorrection (b) PWM-ΣΔ.

In an integral approach the digital PWM generator is used as quantizer in a ΣΔ loop yielding a PWM-ΣΔ loop as shown in figure 8(b). A disadvantage of this approach is that the entire loop needs to run at the high bit-clock frequency.

Essentially, with both approaches any required SNR and THD can be achieved at the expense of higher clock rates as long as the signal remains in the digital domain. Actually, even without correction of output stage errors open loop class-D amplifiers can have very good performance [8,12] provided that an accurate regulated power supply is used. Because of the lack off power supply rejection open loop class-D amplifiers are invariably BTL such that at small modulation depths supply variations largely cancel out.

Some attempts have been made to improve power supply rejection by sensing the supply voltage with a DAC and using feed forward correction of the digital PWM signal, but these designs only yield a moderate improvement in power supply rejection [13,14]. Open loop class-D amplifiers can be found mainly in consumer electronics such as television sets and home-theatre systems.

B. Closed Loop Architectures

An evident way to improve power supply rejection is to apply feedback. Since the output signal of a class-D amplifier is essentially analog most feedback class-D amplifiers require an analog input signal. Closed loop class-D amplifiers can be either *self-oscillating* or *fixed-carrier* based.

1) Delay Based

A basic self-oscillating class-D feedback loop is the delay based loop shown in figure 9. The oscillating frequency f_{PWM} of the loop is expressed as:

$$f_{PWM} = \frac{1-M^2}{4 \cdot T_D} \tag{2}$$

where T_D is the delay time and M is the modulation depth. From (2) can be seen that the switching frequency drops to zero at large modulation depth.

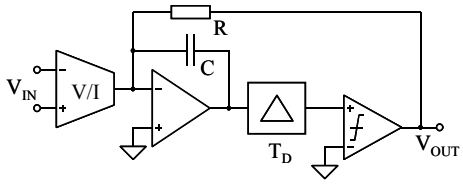

Figure 9. Delay based self-oscillating class-D feedback loop.

An elegant variation on this topology is described in [15] where the demodulation filter is incorporated in the feedback loop. A delay based self-oscillating class-D amplifier is always stable. The loop transfer is expressed as.

$$A\beta(f) = \frac{2}{\pi}\frac{f_{PWM}}{f} \tag{3}$$

From (3) it can be seen that the unity-gain frequency of the feedback loop is coupled to the PWM switching frequency f_{PWM}. This is a common characteristic of class-D feedback loops. Because self-oscillating loops have a variable switching frequency it is not straightforward to increase the order of the feedback loop to achieve higher loopgain.

2) Hysteretic

In a hysteretic class-D feedback loop as shown in figure 10 the output of the loop integrator is constrained within a hysteresis window. The oscillating frequency f_{PWM} of the loop is expressed as:

$$f_{PWM} = \frac{1-M^2}{4 \cdot h \cdot RC} \tag{4}$$

where h is the ratio between the hysteresis window and the supply voltage, RC is the time constant of the integrator and M is again the modulation depth.

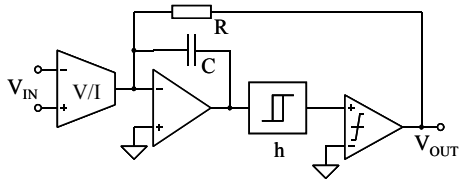

Figure 10. Hysteretic self-oscillating class-D feedback loop.

At first glance the hysteretic loop appears similar to the delay based loop but they are actually very different when comparing both loop transfers. This is because the hysteresis forces the average value of the integrator output to zero creating a virtual ground for low frequencies. The result is a second order loop transfer:

$$A\beta(f) = \frac{12}{\pi^2}\left(\frac{f_{PWM}}{f}\right)^2 \tag{5}$$

Note that the unity-gain frequency of this loop transfer is actually higher than the PWM switching frequency f_{PWM}. Unfortunately the loop transfer of hysteretic loops collapses when a delay is introduced in the loop. For large delays the loop transfer of the hysteretic loop converges to that of a delay based loop. Still for modest (realistic) delays the loop transfer of hysteretic loops is always higher than for any other feedback topology, especially at the higher audio frequencies. Very good performance has been reported on discrete hysteretic amplifiers aimed at high-end audio [16]. A hysteretic ΔΣ class-D amplifier with discrete-time PWM output with very impressive performance is presented in [17].

The main drawback of self-oscillating class-D amplifiers is the variable switching frequency. In multi-channel systems differences in switching frequency can cause audible inter-modulation products known as beat tones. Also when the switching frequencies of two channels are nearly equal they tend to lock onto each other, deteriorating the performance. The variable switching frequency is sometimes presented as an EMI advantage since it distributes energy over a range of frequencies [17] but in practice many equipment builders prefer the predictability of fixed carrier class-D amplifiers.

3) Fixed-Carrier

Figure 11(a) shows a fixed-carrier class-D feedback loop where a triangular reference wave V_{REF} is applied at the inverting input of the comparator creating an NPWM generator. The loop transfer of the fixed-carrier feedback loop is expressed as:

$$A\beta(f) = \frac{1}{\pi}\frac{f_{PWM}}{f} \tag{6}$$

The unity gain frequency is lower than that of self-oscillating loops but because the carrier frequency is fixed it is rather straightforward to upgrade the feedback loop to second order for low frequencies as shown in figure 11(b). In this topology the second integrator both increases the loop order and facilitates generation of the reference triangle V_{REF} [7].

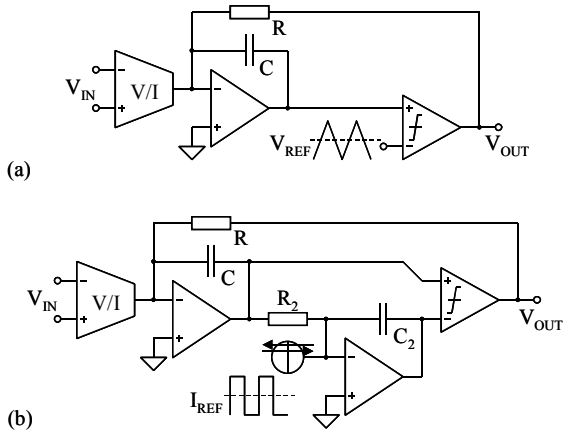

Figure 11. Fixed-Carrier class-D feedback loops (a) 1st order (b) 2nd order.

4) Direct Pulse Amplification

The feedback loops shown in figure 11 can be readily modified to accept a PWM instead of audio input signal by deleting the reference signal. In [18] a class-D amplifier is presented where a feedback loop similar to the one shown in figure 11(b) is driven directly by a bitstream coming from a fifth order noise-shaper running at $64f_s$. Using a digitally generated PWM signal instead has the advantage that the average switching frequency is both reduced *and* constant.

For stability the closed loop gain g needs to be higher than unity to guarantee that the PWM input signal always dominates the feedback. Consequently the modulation depth of the PWM input signal is multiplied by a factor g at the output. The PWM input signal is effectively analog and needs to be well defined in both amplitude and timing. When the PWM source is digital this requires low-jitter re-sampling or, in other words, a high quality one-bit DAC.

V. Power Stage Design

It is a common misconception that *dead time* is required to avoid the occurrence of shoot-through currents in class-D power stages. In [19] it is shown that a proper design of the gate driver circuits is both necessary and sufficient.

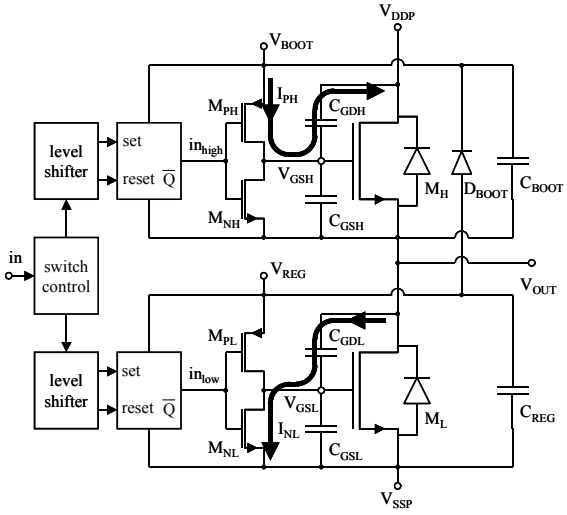

Figure 12. Typical class-D output stage configuration.

In figure 12 a typical class-D output stage is shown in more detail. Two very large DMOS power transistors M_L and M_H are used as switches. Usually n-type power transistors are preferred because they have a lower R_{on}Area product, requiring less area for a given on-resistance, but also complementary output stages are feasible [20]. The backgate diodes of the DMOS transistors serve as fly-back diodes. The lowside gate driver uses an externally decoupled supply V_{REG}. The highside gate driver is supplied from an external capacitor C_{BOOT} that is bootstrapped to V_{REG} with a diode D_{BOOT}. The switching of the output is controlled by a logic circuit *switch control* that communicates with the drivers through high-speed levelshifters [19,8,20]. As can be seen in figure 12, two (identical) inverters $M_{PH/NH}$ and $M_{PL/NL}$ drive the gates of the power transistors M_H and M_L. The dimensions of these inverters together with the parasitic capacitances of the power transistors determine the dynamic behavior of the class-D output stage.

Figure 13 shows some typical waveforms that occur during a rising transition at the output V_{OUT}. The top graphs show the gate-source voltages V_{GSL} and V_{GSH} of the power transistors M_L and M_H respectively. The bottom graph shows the output voltage V_{OUT} and the drain currents I_{DL} and I_{DH} of the power transistors M_L and M_H respectively. The inductor in the demodulation filter forces the output current I_{OUT} to remain nearly constant during output transitions. The output current I_{OUT} can be flowing either towards or from the output stage yielding two scenarios called *soft switching* and *hard switching*.

1) Soft Switching

In case the output transition is supported by the output current this is called soft switching. For a rising output transition this occurs when the output current I_{OUT} flows towards the class-D output stage as shown in figure 13(a). Initially, the lowside power transistor M_L is conducting. Three phases can be distinguished in the transition. Phase I starts when, simultaneously, the input signals in_{high} and in_{low} of both gate drivers change state turning on M_{PH} in the highside and M_{NL} in the lowside. Consequently, the gate of the lowside power transistor M_L is discharged with a current I_{NL} that is proportional to the size of M_{NL}. At the same time the gate of the highside transistor M_H is charged with a current I_{PH} that is proportional to the size of M_{PH}. As soon as V_{GSL} approaches the threshold voltage V_T, the output current I_{OUT} pulls the output node V_{OUT} up entering phase II. During the transition the gate-source voltage V_{GSL} stalls and the discharge current I_{NL} flows almost entirely through lowside gate-drain capacitance C_{GDL}. The slope of the output V_{OUT} is now approximately:

$$\frac{dV_{OUT}}{dt} \approx \frac{I_{NL}}{C_{GDL}} \tag{7}$$

This slope imposes a current equal to I_{NL} through the highside gate-drain capacitance C_{GDH}. This pushes the gate-source voltage V_{GSH} down under the *mandatory* condition that I_{PH} is smaller than I_{NL}. After the transition phase III starts and the charging of the gate of the highside power transistor M_H is resumed. Remarkably, the currents I_{DL} and I_{DH} through the power transistors hardly change during the output transition but change very abruptly afterwards.

2) Hard Switching

In case the output current resists the output transition this is called hard switching. For a rising output transition this occurs when the output current I_{OUT} flows out of the class-D output stage as shown in figure 13(b).

The start of phase I is identical to the soft switching scenario. As V_{GSH} reaches the threshold level the drain current I_{DH} of highside power transistor M_H starts to build up while the drain current I_{DL} of the lowside power transistor M_L starts to decrease. The sum of these currents equals the output current I_{OUT}. The output node V_{OUT} sticks to the lowside while V_{GSH} increases further until the current I_{DH} through M_H matches the output current I_{OUT}. At this moment the current through the lowside power transistor M_L is zero and one would expect the output node V_{OUT} to start the transition immediately. However the drain current I_{DH} of the highside power transistor M_H keeps increasing while the current through the lowside power transistor M_L reverses. This happens because there is still minority charge left in the backgate diode that needs to be flushed out. This mechanism, known as *reverse recovery* is probably the most important source of EMI in class-D amplifiers. When the backgate diode finally runs out of minority carriers the reverse recovery current stops abruptly causing the output transition to start at an accelerated pace.

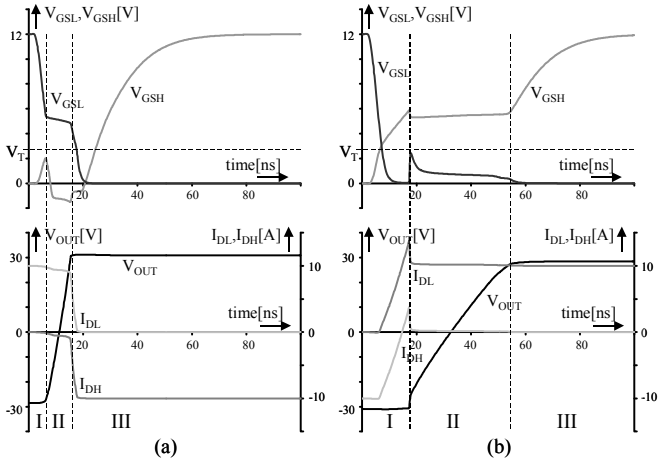

Figure 13. Rising output transition (a) soft switching (b) hard switching.

Subsequently, feedback through the gate-drain capacitance C_{GDH} causes V_{GSH} to be pushed down causing a characteristic 'overshoot' in V_{GSH}. Also the gate of the lowside power transistor M_L is pulled up which can lead to additional peak current if the threshold voltage V_T is exceeded. After this rapid start the transition continues at a more moderate pace during in phase II. During the transition the gate-source voltage V_{GSH} stalls and the charge current I_{PH} flows almost entirely through gate-drain capacitance C_{GDL}. The slope of the output node V_{OUT} is now approximately:

$$\frac{dV_{OUT}}{dt} \approx \frac{I_{PH}}{C_{GDH}} \tag{8}$$

This slope imposes a current equal to I_{PH} through the lowside gate-drain capacitance C_{GDL} that attempts to pull up the gate of the lowside power transistor M_L. To prevent M_L from turning on discharge current I_{NL} needs to be sufficiently larger than I_{PH}. Because the charge current I_{PH} is smaller than the discharge current I_{NL} the slope of the hard switching transition is less steep than during soft switching. After the transition the charging of the gate of highside power transistor M_H is finalized in third phase III.

VI. Design Examples

High power class-D amplifiers have become standard in many consumer electronic applications such as television sets and home-theatre systems. Currently, class-D is also making a cautious entrance into the automotive domain. The first integrated class-D audio amplifiers designed to operate directly from the car battery are now entering the market. A third domain where class-D is emerging is in mobile applications such as cellular phones and MP3 players. In these

applications the output power is low, e.g. around 1W, so not heat production but extension of battery life is the driver behind class-D.

Class-D amplifiers for both consumer and automotive applications are typically made in dedicated high-voltage technologies [21]. For mobile applications standard CMOS technologies are preferred. Although conceptually similar, class-D amplifiers in the different application domains have to deal with rather different environments.

A. Consumer Electronics

The high volume consumer electronics market is very much cost driven. Moreover there is a tendency towards higher output power and more channels. A major concern with high power class-D amplifiers is robustness. Switching a current of 10A from a 60V supply rail is no trivial matter. During hard switching the peak dissipation in the power transistors easily exceeds 600W. Also, because of extremely high dI/dt's in the supply lines during soft switching the influence of parasitic inductances need to be taken into account. The voltage excursions that occur at the supply terminals can easily exceed the breakdown voltage of the power transistors causing permanent damage.

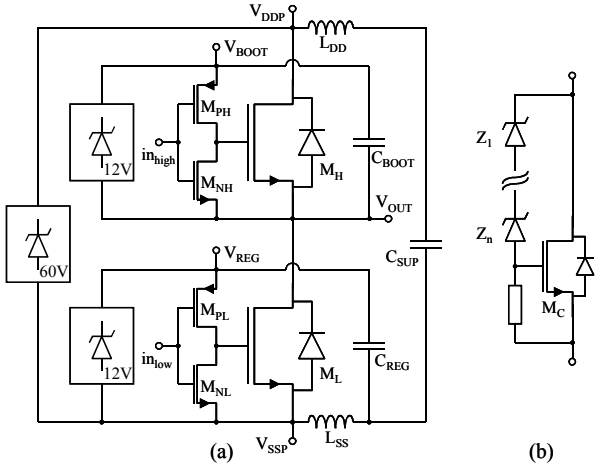

Figure 14. (a) parasitic inductances and voltage clamping (b) active clamp

However, the Achilles heel is the lowside driver because the external decoupling capacitor C_{REG} is in series with inductance L_{SS} as shown in figure 14(a). Consequently, the negative voltage excursions at the source of the lowside power transistor M_L appear directly across the lowside driver circuits that typically have a lower voltage rating. Creating headroom by raising the breakdown voltage would also increase the R_{on}Area product and consequently chip area.

An effective way to prevent damage to the circuits is the use of active voltage clamps as shown in figure 14(b) where a reasonably large transistor M_C is turned on when the voltage across the terminals exceeds a limit that is determined by the number of Zener diodes in the stack and can be tuned to match the breakdown voltage of power transistors. In this way power transistors can be used with a minimal overhead in breakdown voltage.

B. Automotive

Audio amplifiers aimed at automotive applications are very similar to those for consumer electronics but demands on robustness and EMI are more stringent. Automotive audio amplifiers are supplied directly from the 14.4V car battery and have a BTL configuration by default in order to get enough output power. However, open loop amplifiers are unacceptable since the battery voltage is rather noisy. In addition to supply noise the amplifier needs to deal with extreme supply voltage excursions. During *engine start* the battery voltage can drop from 14.4V to 6V while the amplifier needs to continue playing without causing audible artifacts. When the battery is disconnected while the engine is running *load dump* occurs causing the supply voltage to surge up to as high as 50V. Since the audio amplifier is supplied directly from the battery it needs to be capable of surviving this condition. This leads to a different clamping strategy to limit inductive voltage peaking compared to the high voltage designs in consumer applications. In terms of area it is more economical to use power transistors with a lower breakdown voltage and distribute the load dump voltage between them. In that case it is not possible anymore to use a central active clamp as shown previously. Instead a separate clamp is added parallel to each power transistor with an ignition voltage below the breakdown voltage of the power transistors as shown in figure 15.

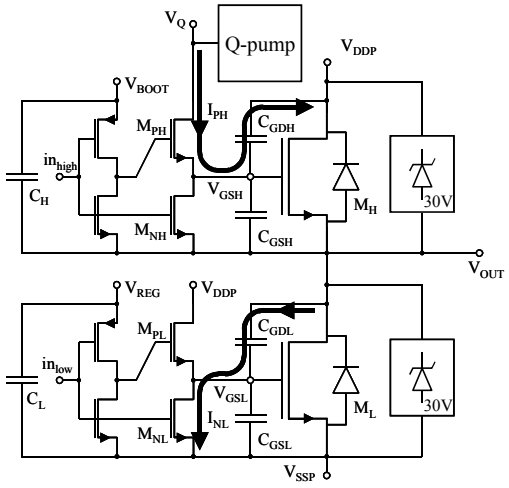

Figure 15. Automotive class-D output stage

As can be seen also the gate driver topology is different. This is because the preferred format for automotive amplifiers is the four-channel quad. When using external bootstrapping this adds up to eight external capacitors requiring eight pins. Therefore it makes sense to use a single externally decoupled charge-pump to generate the drive voltage for the highside power transistors. The voltage slope at the output during hard switching transitions is now controlled by the gate-drain capacitance $C_{GDL,GDH}$ of the power transistors and the g_m of the source followers $M_{PL/PH}$. The inverters driving the source followers $M_{PL/PH}$ can be decoupled with small on-chip capacitors $C_{L/H}$.

C. Mobile

The need for class-D amplifiers in mobile applications is driven by the demand for longer battery life and again more output power. Three product types can be seen where class-D is emerging.

Class-D amplifiers are being integrated in audio codecs that are part of large mixed-signal SoC's where GSM baseband and audio interfaces (ABB) are combined [22]. A block diagram of such an audio codec, shown in figure 16. contains multiple analog microphone and line inputs and analog speaker, headphone and line outputs. These complex systems are typically realized in advanced deep submicron CMOS technologies.

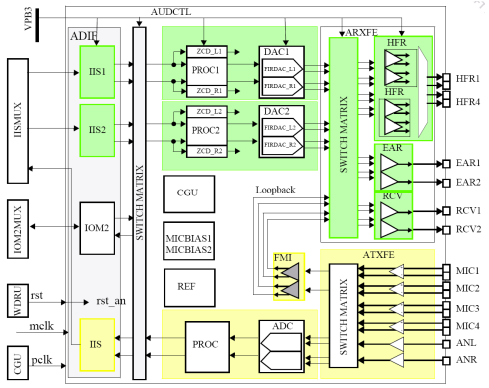

Figure 16. Audio codec in typical ABB system.

In direct competition with the ABB are power management units (PMU) that can be found in cellular phones but also many other portable applications such as PDA's and MP3 players. Such PMU chips are often made in dedicated CMOS technologies with high voltage capabilities that facilitate the realization of switch-mode DC/DC converters that are akin to class-D amplifiers. These technologies are generally better suited for the implementation of class-D amplifiers and a convergence of PMU with audio codecs is ongoing. Besides integration in ABB or PMU there is a significant market for stand-alone class-D amplifiers.

Output power for speaker drivers in mobile applications is typically in the range from 500mW to 1W. The output stage is preferably connected directly to the battery [23]. This battery voltage ranges between 2.5V and 4.5V and can even be as high as 5.5V during charging. A high power supply rejection is essential especially in cell phones because the battery voltage is polluted by the characteristic 217 Hz interval of the transmit power amplifier. Consequently, class-D amplifiers with feedback are preferred. A key feature in mobile class-D amplifiers is filterless operation. In a BTL amplifier that uses BD-modulation the amount of differential mode high frequency energy is reduced compared to AD-modulation. In this case the speaker itself can act as filtering element provided that the speaker is close to the amplifier output.

Class-D amplifiers in mobile applications are typically realized in standard CMOS technologies. The maximum allowed voltage between the device terminals is usually much lower than 5.5V. In this case cascodes can be used to distribute voltage between devices. A simplified cascoded class-D power stage is shown in figure 17.

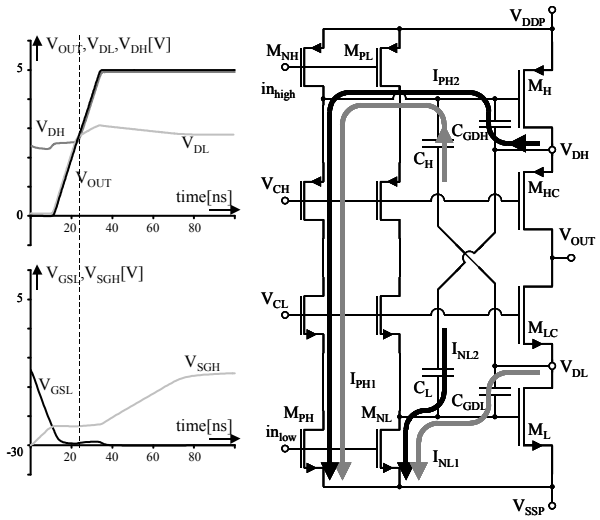

Figure 17. Cascoded class-D output stage for direct battery hookup.

The highside PMOS transistors do not require bootstrapping. The cascodes $M_{LC/HC}$ are biased such that when the corresponding power transistor is switched off the supply voltage is distributed evenly. To maintain slope control during the output transitions two capacitors $C_{L/H}$ are added that match the gate-drain capacitances $C_{GDL/GDH}$ of the power transistors $M_{L/H}$. During the first half of a rising edge transition the lowside cascade M_{LC} is in the linear region while the highside cascade M_{HC} is off. In this case the voltage V_{DL} at the drain of power transistor M_L follows the output voltage V_{OUT} and the voltage slope is determined by current I_{PH1} and capacitor C_H. During the second half M_{HC} is in the linear region and M_{LC} is off. In this case the voltage V_{DH} at the drain of the highside power transistor M_H follows the output voltage V_{OUT} and the voltage slope is determined by the current I_{PH2} and gate-drain capacitance C_{GDH}.

D. Headphone amplifiers

Headphone amplifiers are typically stereo SE with a common return line. Operation from a single supply rail is realized with AC-coupling as shown in figure 18(a). Typical output power ranges from 10mW to 100mW.

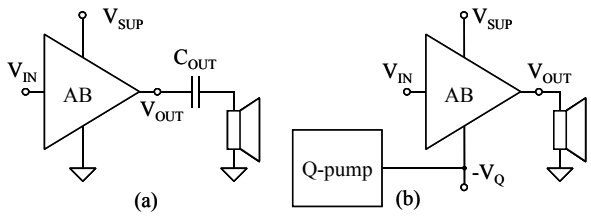

Figure 18. Headphone amplifiers (a) AC coupled (b) True ground

At such low output power there is not much to be gained by using class-D. Besides, the relatively long cable that is usually connects to the headphone excludes the possibility of filterless operation. Instead the current trend is class-AB with a negative supply rail to enable so-called true ground

application as shown in figure 18(b) that eliminates the coupling capacitor C_{OUT}. Because of the modest power requirements the negative supply voltage can be generated with a charge-pump circuit.

VII. Digital To Analog Conversion

High-end audio DACs [24] have distortion figures better than 100 dB, a resolution of 16 bit or more and a dynamic range of more than 100 dB in the audioband. Older designs have 16 to 18 bit resolution, 2 to 4 times oversampling and binary weighted current sources to make the output signal. The high precision is realized by trimming or Dynamic Element Matching (DEM) techniques [25,26]. Later designs use high oversampling rates (128, 192, 256f_s) and low resolution (1-5bits). The resulting quantization noise is suppressed in the audioband by aggressive noise shaping in the digital front-end of the (ΣΔ) DAC. The out-of-band noise must be attenuated to a level lower than -60 dB by an analog low-pass filter or by Finite Impulse Response (FIR) filtering in the DAC output [27]. Both switched-current continuous-time (CT) and switched-capacitor (SC) outputs are used. The demands on the analog precision of the output circuit are high. In one-bit DACs the clock jitter must be extremely low and the symmetry of the rising and falling edges of the output signal must be near perfect to limit the effect of Inter Symbol Interference (ISI). In multi-bit DACs the accuracy of the DAC elements must be very high as it determines the linearity of the converter. DEM techniques like DWA are used to improve on this. The tolerance to clock jitter is better because the steps in the output signal are smaller.

A. D/A Conversion for closed-loop Class-D Amplifiers

Audio signal sources are dominantly digital while class-D (and class-AB) audio amplifiers are fundamentally analog. Although PWM signals can be generated in the digital domain it is not self-evident to maintain the signal quality in the power output stage of the class-D amplifier. This quality depends on the precision of the edges of the class-D output stage and the stability of the supply voltage. Therefore class-D amplifiers with analog feedback are preferred having better audio performance at lower cost. However, the input signal must be analog so a DAC is needed in front of the class-D amplifier. Most modern audio DAC solutions have an output signal that still contains considerable out-of-band noise. The combination of DAC with closed-loop class-D amplifiers requires dedicated architectures to avoid intermodulation of out-of-band quantization noise back into the audio band [28,29].

An attractive D/A architecture for combination with class-D amplifiers is a digital PWM modulator followed by a FIRDAC as shown in figure 19. A FIRDAC performs D/A conversion and lowpass filtering simultaneously. The advantage of using a digital PWM signal instead of a bitstream from a one-bit ΣΔ modulator is the transition rate is signal independent. Due to the fixed transition rate that is inherent to PWM signals, distortion caused by ISI is eliminated completely. Digital audio PCM signals have a high resolution ranging from 16 to 24 bits. To convert of a high resolution PCM signal to a digital PWM signal without degrading signal quality a number of digital signal processing steps is needed. Starting from a 16-bit non-oversampled (1f_s) input signal, for example from a CD player, upsampling and interpolation is needed to get to a convenient PWM frequency. The first stage performs 8 times upsampling to 8f_s and is then lowpass filtered to remove the aliases.

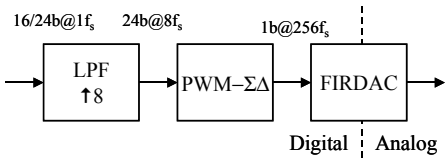

Figure 19. PWM ΣΔ FIRDAC

A 16 bit resolution in the pulse width would require a unpractical high clock frequency of 23 GHz. Therefore the signal is truncated to 4-bit PWM resolution in a PWM-ΣΔ noiseshaper resulting in a 256f_s PWM bitstream with a 16f_s transition rate. The PWM signal still contains a lot of out-of-band quantisation noise. This noise attenuated effectively by the FIRDAC structure.

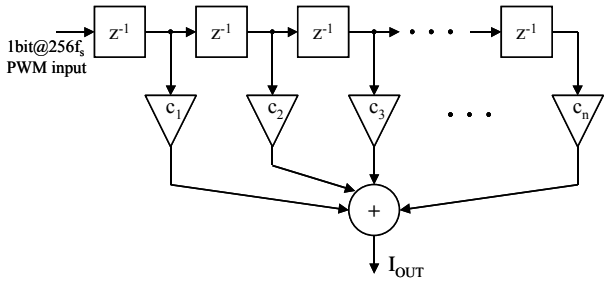

Figure 20. FIRDAC block diagram

A block diagram of the FIRDAC is shown in figure 20. It consists of a digital delayline for the PWM bitstream. Each delayline tap is connected to a one-bit DAC. Each one-bit DAC is a switchable differential current source. The value of the current is proportional to the coefficient value that is needed to get the intended filter characteristics. An important observation is that all separate one-bit DACs work in parallel. Since a one-bit converter with a PWM bitstream input produces no distortion, the summation of the independent output signals does not add any distortion by itself either. The filtering comes from the summation of delayed (and weighted) versions of the same output signal. Errors in the coefficient weight factors only influence the filter characteristic, mainly in the stopband. To attenuate the out-of-band noise to less than -60dB an averaging Hamming filter with 320 coefficients is used. The FIRDAC solution not only shows high attenuation of the out-of-band noise, it also produces an output signal with very small output steps. Because of these small steps the FIRDAC is quite insensitive to clock jitter. For 110dB SNR in the audioband the clock jitter can be as high as 6ns whereas a one-bit converter needs a clock jitter of a few picoseconds for the same SNR.

The chip area of a FIRDAC depends on the required coefficient accuracy that determines the stopband attenuation. The SNR increases with higher DAC output currents because the gate-source voltage of the current source transistors

increases leading to a more optimal biasing for noise. Details about noise and filter optimization can be found in [30]. From this article it can be concluded that the FIRDAC area scales down considerably with improving lithography and thinner gate oxide. The PWM-ΣΔ FIRDAC is not only favorable in combination with class-D amplifiers. Besides being tolerant to jitter and ISI the PWM-ΣΔ FIRDAC is generally insensitive to signal dependent disturbances. This facilitates portability of design and makes the PWM-ΣΔ FIRDAC very attractive as general-purpose audio DAC.

VIII. Conclusion

Employing a continuous-time input filter in a traditionally favored switched-capacitor audio ΣΔ modulator overcomes the input sampling switch non-linearity that becomes more problematic at lower supply voltages. MASH ΣΔ converters and multi-bit A/D and D/A architectures incorporating data weighted averaging algorithms achieve excellent linearity and suffer much less from idle channel tones compared to a single-loop one-bit ΣΔ modulator.

Class-D amplifiers are largely replacing class-AB in most application areas. Fixed-carrier closed loop architectures are widely preferred mainly because they have good power supply rejection. Different application domains result in different topologies for the output stage but the switching dynamics remain essentially the same.

The PWM-ΣΔ FIRDAC is an attractive D/A architecture especially for combination with class-D amplifiers because it offers good out-of-band noise suppression and high linearity.

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