Pipelined A/D converters

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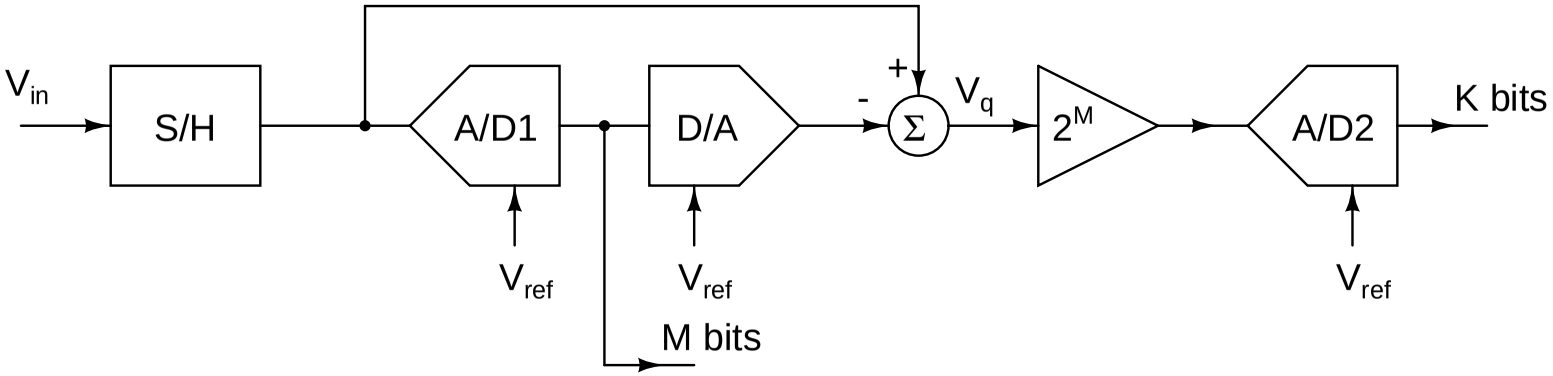
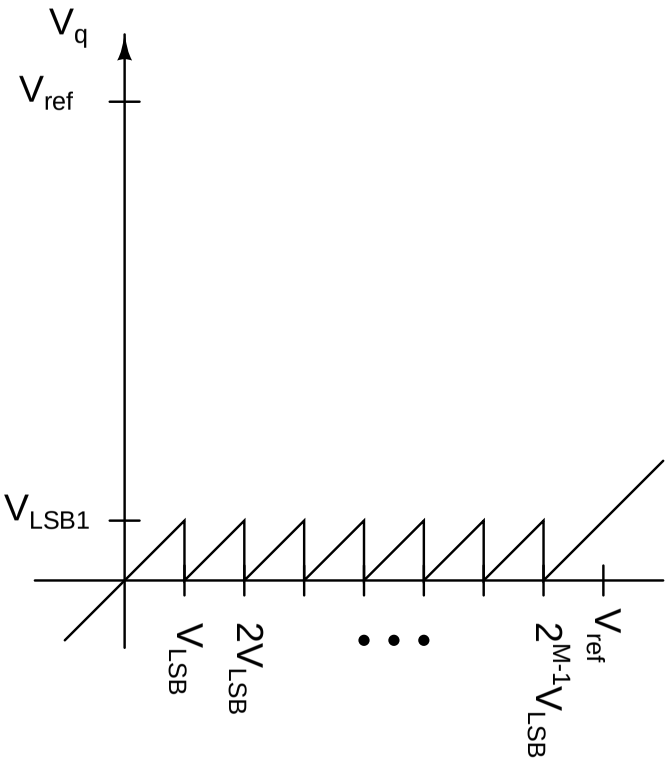
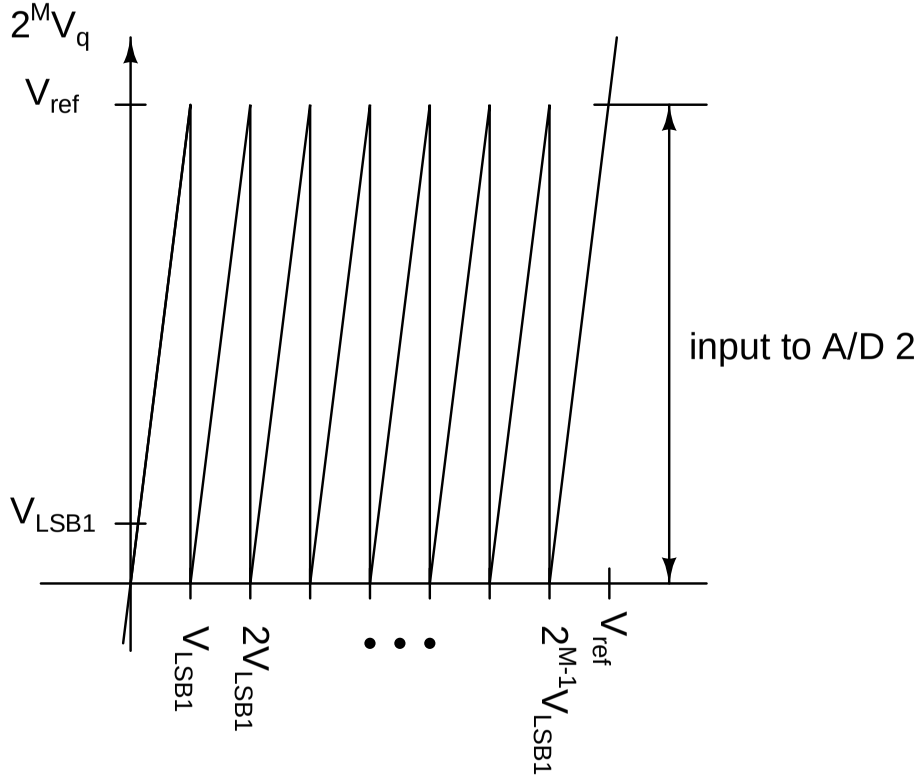
OUTLINE

- Two step A/D converter
- Two step A/D converter with digital correction
- 1.5 b/stage pipelined converter with digital correction

Two step flash converter



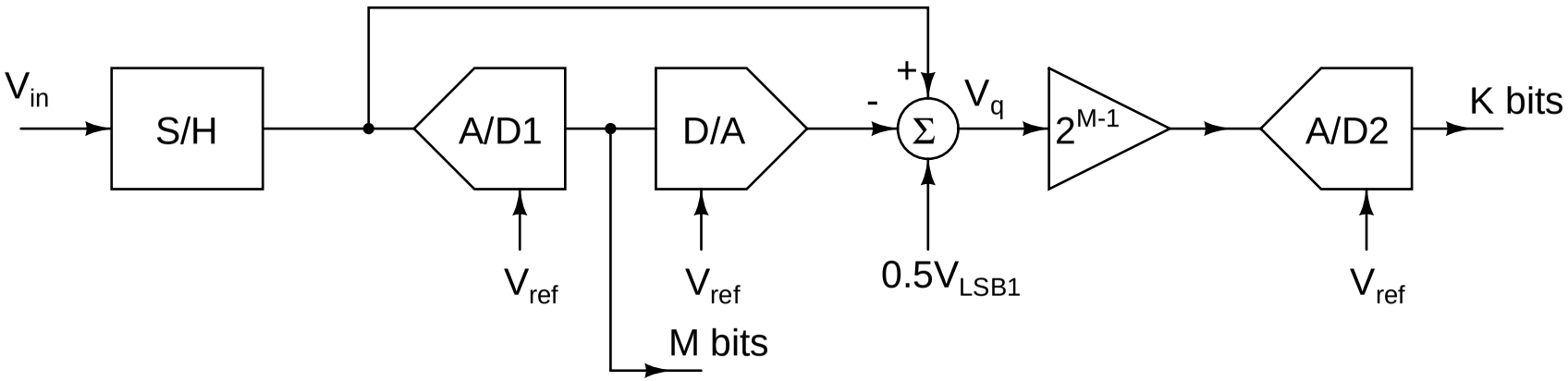


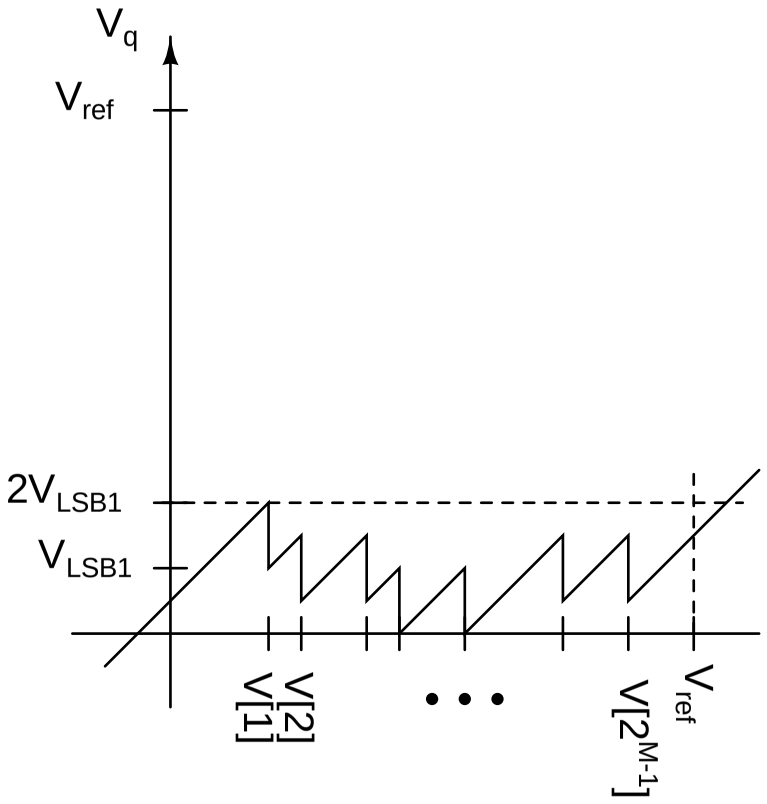


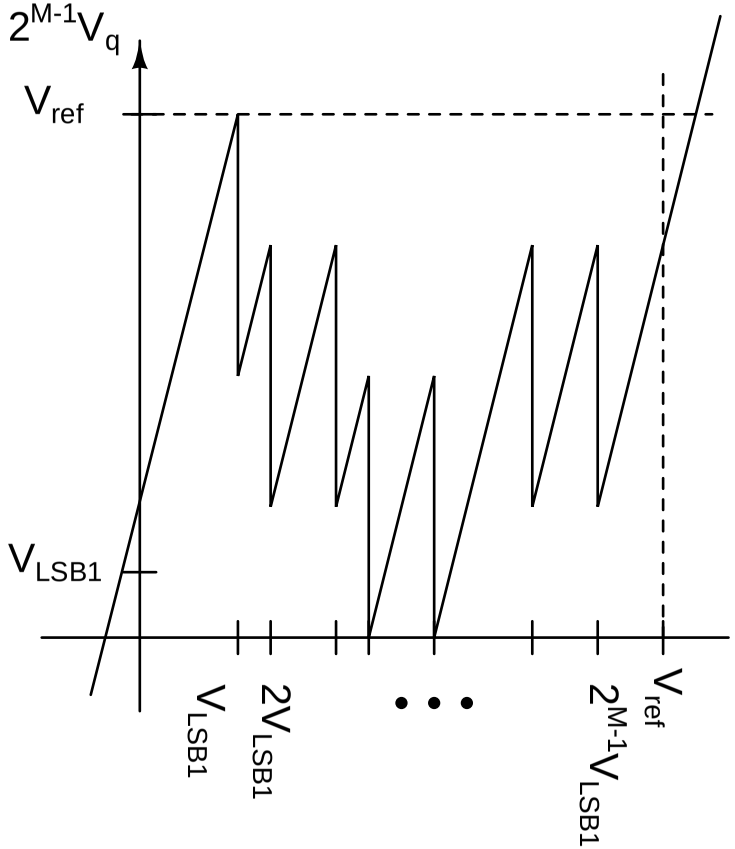
Two step flash converter

- A/D 1 quantizes the input to M bits
- Ideally, $0 \leq V_q \leq V_{LSB1}$ ($V_{LSB1} = V_{ref}/2^M$)
- A/D 2 quantizes the amplified residue ($2^M V_q$) of A/D 1 to K bits
- A/D 1 needs to be accurate to $N = M + K$ bits, A/D 2 to K bits. See HW4 solutions for detailed calculations.
- Overal resolution is $N = M + K$ bits. A/D 1 provides M bits (MSB), A/D 2 provides K bits (LSB)

Two step flash converter with digital correction







Two step flash converter with digital correction

- A/D 1 quantizes the input to M bits
- With INL=0.5LSB, $0 \leq V_q \leq 2V_{LSB1}$ ($V_{LSB1} = V_{ref}/2^M$)
- Amplify by 2^{M-1} instead of 2^M so that the amplified residue is contained in $(0, V_{ref})$, the range of A/D 2
- A/D 2 quantizes the amplified residue ($2^{M-1}V_q$) of A/D 1 to K bits

Two step flash converter with digital correction

- A/D 2 output can be used to determine if the output of A/D 1 needs correction
  - $0 \leq 2^{M-1}V_q < V_{ref}/4$: reduce A/D 1 output by 1
  - $V_{ref}/4 \leq 2^{M-1}V_q < 3V_{ref}/4$: Use A/D 1 output as is
  - $3V_{ref}/4 \leq 2^{M-1}V_q < V_{ref}$: increase A/D 1 output by 1

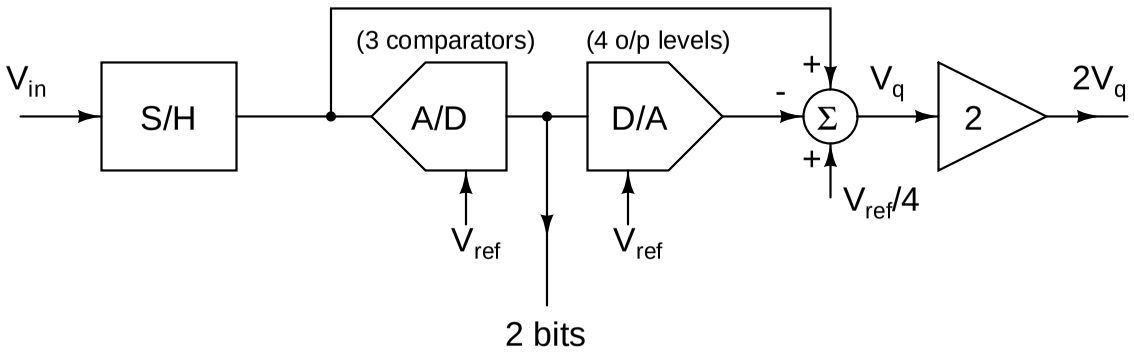
- A/D 1 needs to be accurate to M bits, A/D 2 to $K+1$ bits.

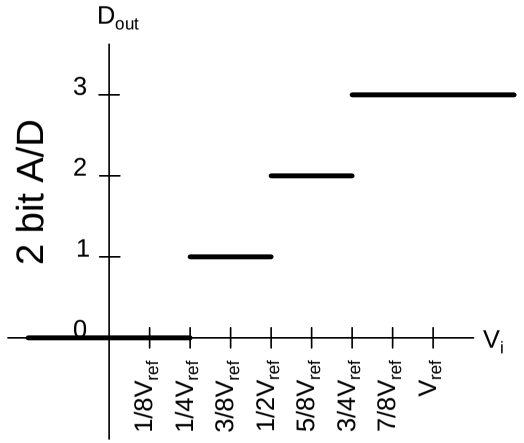
- Overall resolution is $N = M + K$ bits. 1 bit redundancy in A/D 2 helps relax A/D,1 requirements from N bits to M bits. A significant practical advantage. A/D 1 provides M-1 bits (MSB) and A/D 2 provides K+1 bits (LSB).

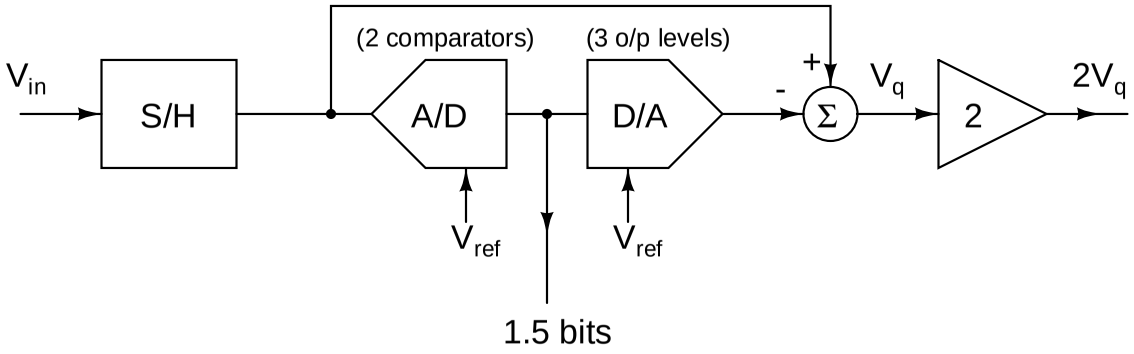
Multi step (pipelined) A/D converter with 1 effective bit/stage

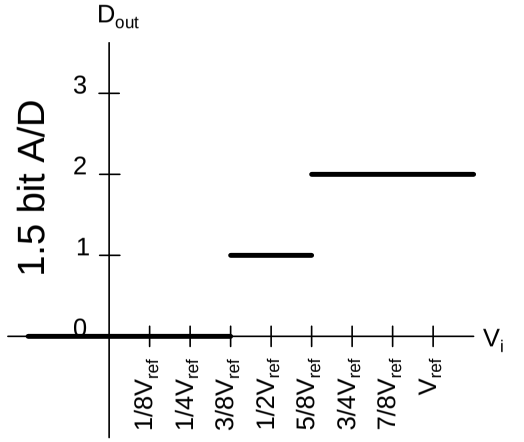
- Having a multi step converter with 1 corrected bit per stage as described above implies 2 bit raw resolution in each stage. This means a 2 bit A/D converter, 2 bit D/A converter and an amplifier of gain 2. It turns out that this is not necessary and a 1.5 bit resolution in each stage provides *exactly* the same effective resolution as a 2 bit resolution in each stage. This leads to significant savings in hardware.

1.5 bits/stage vs. 2 bits/stage: Structure



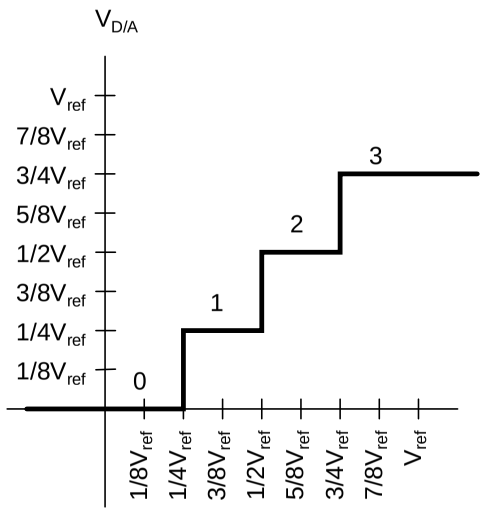




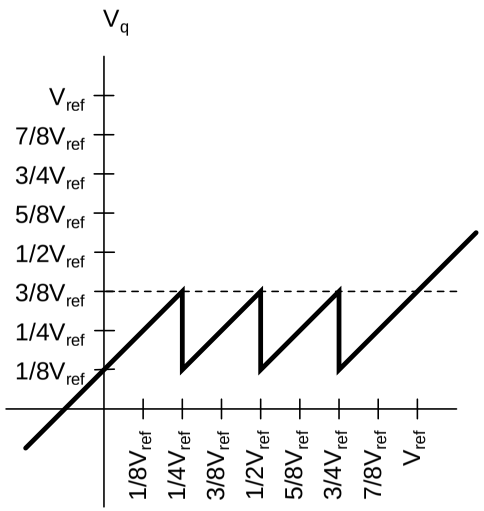


1.5 bits/stage vs. 2 bits/stage: Residue

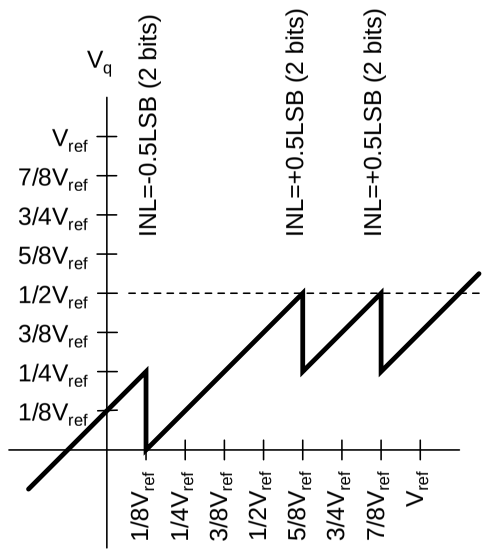
2 bit A/D



A/D characteristics
D/A output

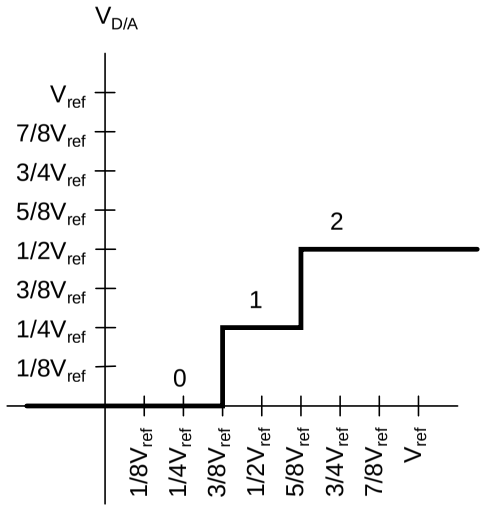


residue, with an ideal A/D

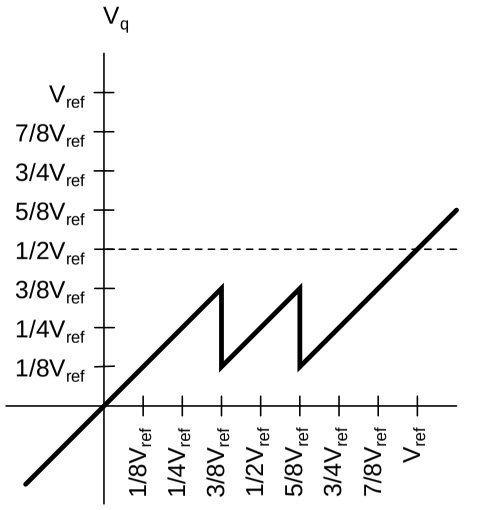


residue, with a nonideal A/D

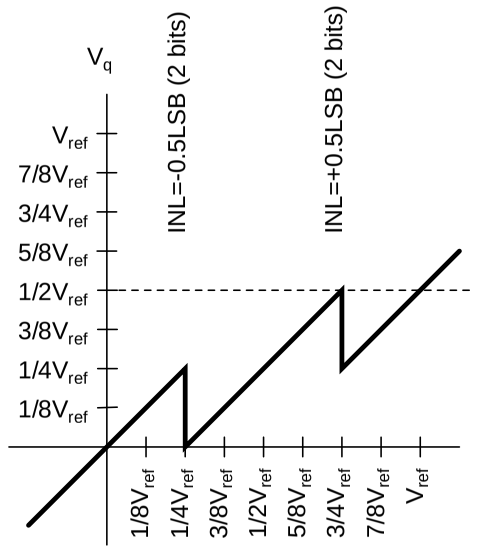
1.5 bit A/D



A/D characteristics
D/A output



residue, with an ideal A/D

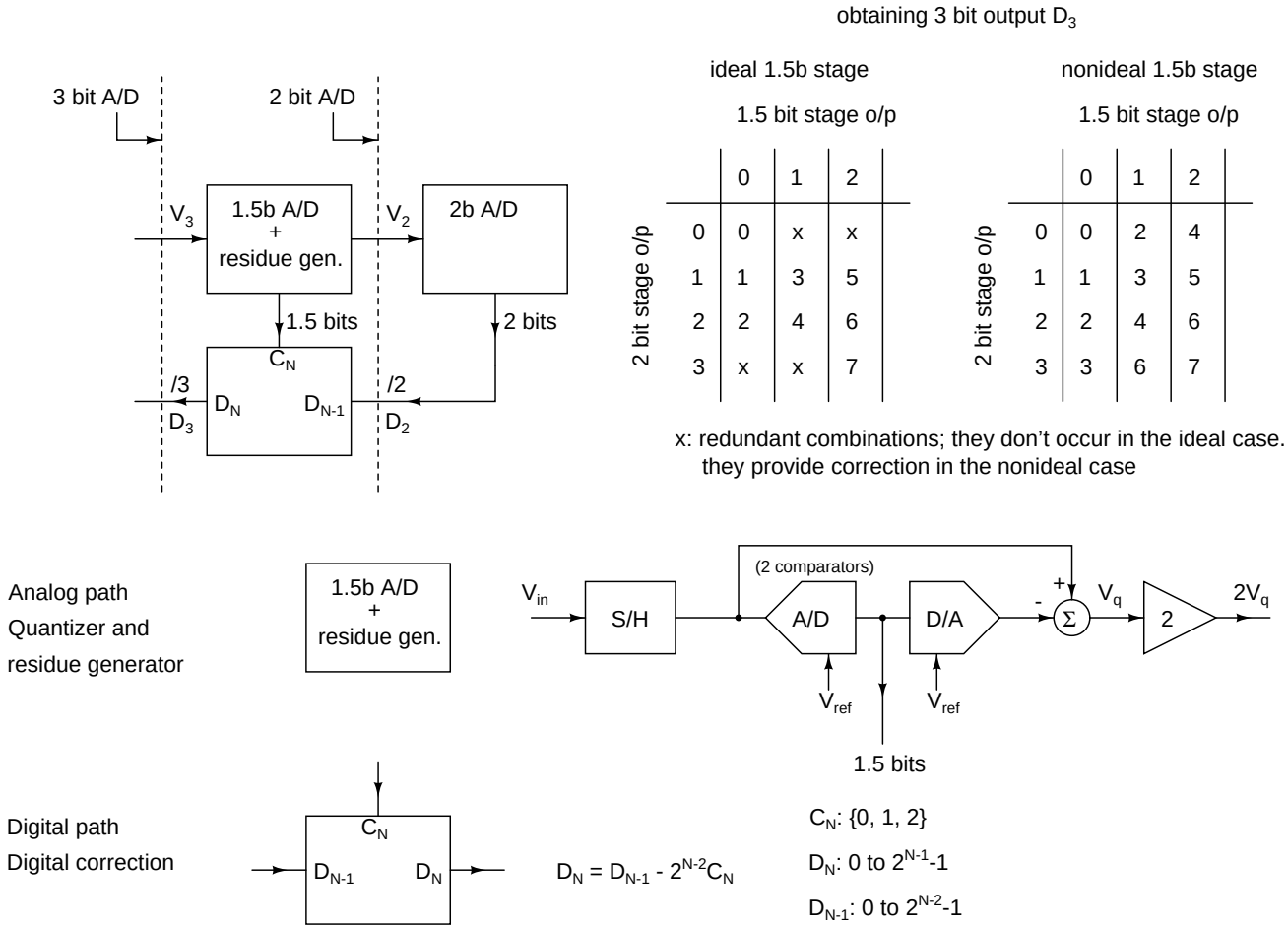


residue, with a nonideal A/D

1.5 bits/stage vs. 2 bits/stage

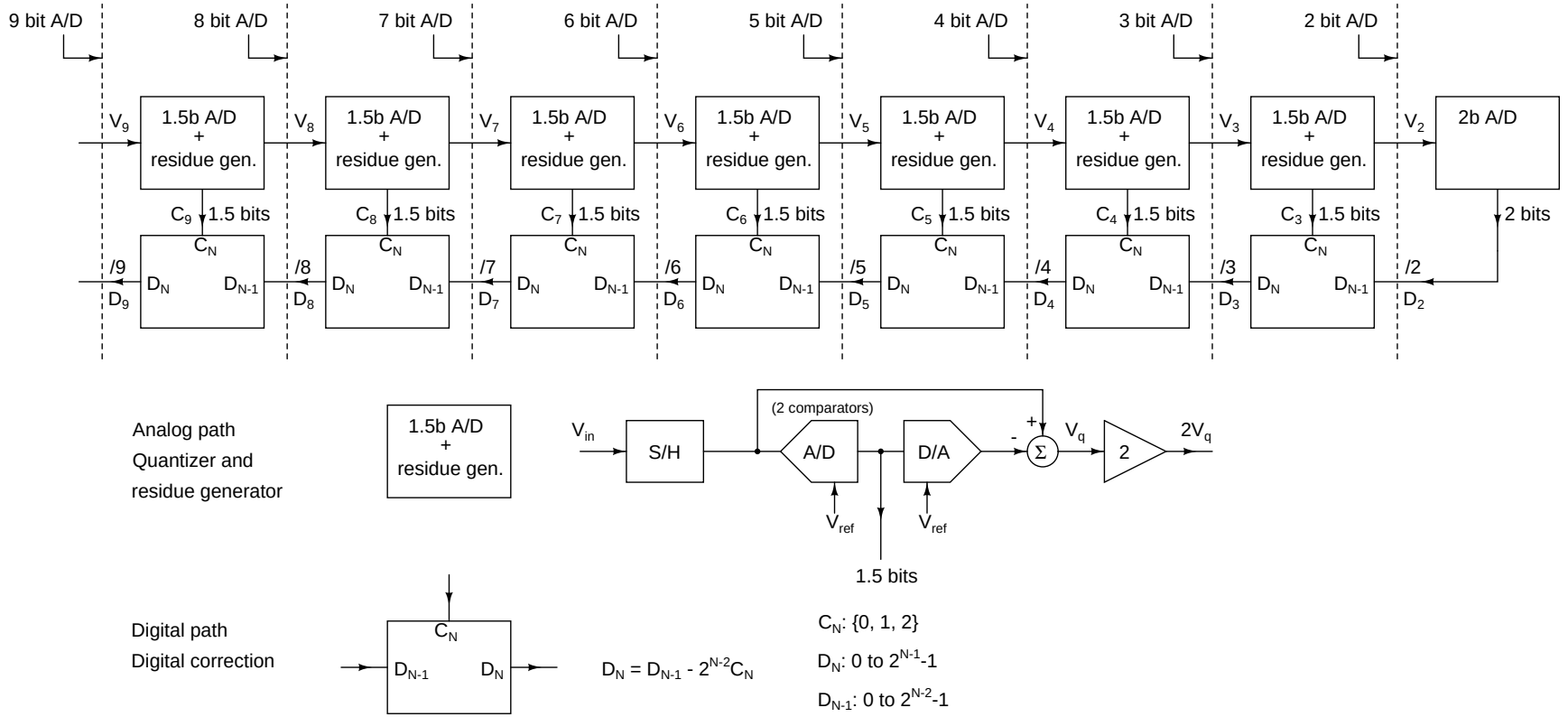
- In the ideal case, having 2 bits per stage has a smaller range of residue than having 1.5 bits/stage
- In the nonideal case (INL $<$ 0.5 LSB at the 2 bit level), having 2 bits per stage and 1.5 bits/stage result in exactly the same range of residues
- Therefore, there is no need to resolve 2 bits. 1.5 bits are enough

Digital correction



- 1.5 b stage is followed by an ideal 2 bit stage. This can be used to obtain 1 effective bit from the first stage.

1.5 b/stage pipelined A/D converter with digital correction



1.5 b/stage pipelined A/D converter with digital correction

- The last stage is not digitally corrected. It has an output D_2 with a 2 bit resolution.
- The last stage provides digital correction to the previous stage. D_2 and C_3 are used to obtain a 3 bit output D_3 corresponding to the analog voltage V_3.
- D_3 and C_4 are used to obtain D_4, the digital representation of V_4 and so on...

1.5 b/stage pipelined A/D converter with digital correction

- The analog residue propagates from the left to the right in the figure. The digitally corrected output propagates from the right to the left.
- Digital delays are needed to combine the stage outputs (C_N, D_{N-1}) appropriately. These are not shown in the figure.
- If the residue needs one clock cycle to propagate through each stage and the digital correction needs 1 cycle in each stage, the net latency is $\approx 2NT_{clk}$ where N is the resolution of the A/D converter.