

Fall 2004; E6316: Analog Systems in VLSI; HW5

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1.

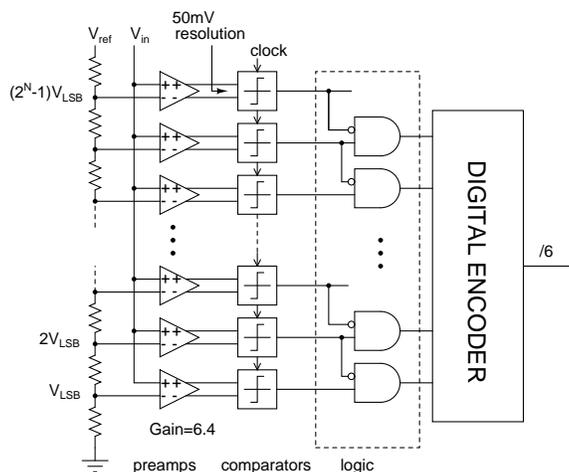


Figure 1:

2. Fig. 1 shows a 6 bit 2 GSamples/s flash A/D converter with $V_{ref} = 1$ V. It has a two input gate array to convert the thermometer code to a “1 of N” code. What is the minimum clock skew that can cause bubble errors? Compare it to the answer for midterm, problem (3).
3. Design the MOS track and hold circuit shown in Fig. 2(a). The load capacitor C_L is 2 pF. The clock is a 1 GHz clock that goes between 0 and 3.3 V. The input varies around a dc level of 0.5 V. Use 3.3 V devices (nch3, pch3) in the library “tsmc025”. Design the MOS switch such that when its terminals are at the input common mode voltage, its resistance results in a time constant that is 10% of the clock cycle. The circuit in Fig. 2(b) can be used to simulate the small signal resistance (with small v_x , of course). Give the size of the device. Simulate the following:
 - (a) Plot the input and output waveforms (overlaid on the same axes) for $f_s = 1$ GHz, $f_{in}/f_s = 9/64$, amplitude $V_p = 0.4$ V. Plot at least one full cycle of the input. Briefly describe different aspects of the waveform.
 - (b) Track to hold mode pedestal. Simulate this using a dc input at the common mode voltage.

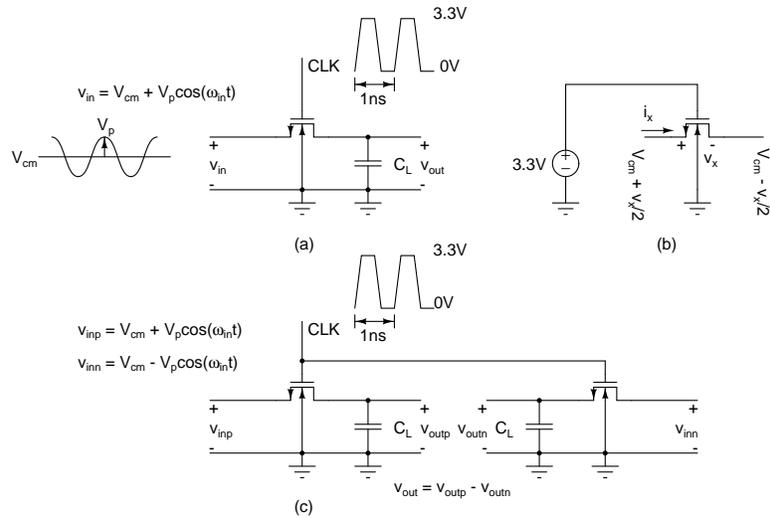


Figure 2:

- (c) Fundamental, 2nd, and 3rd harmonic components¹ for a) $f_s = 1\text{GHz}$, sinusoidal inputs at $f_{in}/f_s = 1/64$ and $f_{in}/f_s = 65/64$, $V_p = 0.1\text{V}$ and $V_p = 0.4\text{V}$ (at each input frequency, simulate for the two specified input amplitudes).

For (b) and (c) above, no need to submit the plots. Just summarize the results.

4. Repeat all the simulations above for Fig. 2(c). How does it compare with the single ended circuit?

¹Use the method described in the handout ‘Simulating the distortion of sample and hold circuits’