E4215: Analog Filter Synthesis and Design
Simulating switched capacitor filters in spectre

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The frequency response of continuous time circuits can be simulated using "ac" analysis in spectre or other spice simulators. The same cannot be done for switched capacitor filters as the circuit functions as intended only when the clocks are operating the switches in the specified manner. The behavior of the circuit at a particular operating point (which is what is simulated in the "ac" analysis) is meaningless.

Fortunately, it is quite simple to simulate the unit sample response of a switched capacitor system. Since the transfer function is related to the impulse response by the fourier transform, the former can then be computed.

Fig. 1(a) shows a general switched capacitor filter. The inputs and outputs are shown in a general form in Fig. 1(b). The input is shown changing with the rising edge of ϕ_1. This is important and should be known beforehand to set up the input correctly in the impulse response simulation. The output voltage is shown changing in both phases, which is true in the general case. It should also be specified which phase the output is taken from. Assume that the output is taken in ϕ_2. It is important to take the output after it has settled to a constant value in that phase.

Fig. 1(b) shows the signals in the measurement of the unit sample response. Since it is specified that the input changes with the rising edge of ϕ_1, the unit pulse is initiated at the rising edge of ϕ_1. The output is specified to be taken in ϕ_2. So the samples for the computation of the sample response are taken as shown, at time t_2 (which is near the end of ϕ_2) and every T_s (sampling period) thereafter. N samples are taken.

The Discrete Fourier Transform (DFT, accessible from the Calculator in Analog artist as "dft") of these N samples is the transfer function of the circuit between input V_{in} and the output V_{out}. Because of the way it is implemented in Analog artist, the dft needs to be multiplied by $N/2$.

Syntax: dft(`Vtest, tstart, tstop, npts, ''Rectangular'', 1, 1`). This gives you the dft of `Vtest` with the first sample at `tstart` and `npts` ($= N$) samples spaced `(tstop-tstart)/npts` apart. Don't change the last 3 arguments of the function. For more extensive documentation, consult cadence help or type `ocnHelp(''dft'')` in Cadence main window.

Take $N = 1024$ or higher. `tstart` is usually zero. You need to simulate long enough to get N points spaces T_s and plot the scaled dft. i.e. plot $N/2*$dft(`Vtest, tstart, tstop, npts, ''Rectangular'', 1, 1`

The schematic **scfcomponents** in **E4215_examples** contains a nonoverlapping cock generator, one half of a switch used in SC circuits, and a unit sample source. The parameter T controls the period. simulate the clock generator and the unit sample source. Modify the source so that it changes on a different clock phase. These components can be used to simulate SC circuits. You will need to change the input pulse position and the position of the sample t_1 depending on the specified input and output timing.

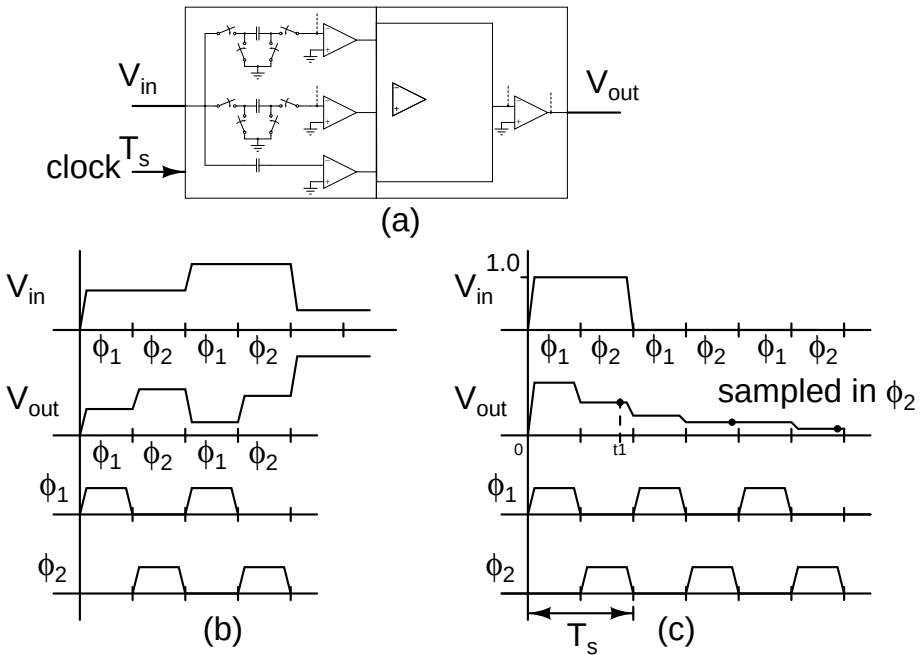

Figure 1: (a) A general switched capacitor filter, (b) General form of inputs and outputs, (c) Setup for impulse response simulation (input changes with **rising edge of** ϕ_1 and the **output is taken in** ϕ_2)