Assignment: #3

Due Date and Time: Mar. 2, 2020, 11:59PM

Topics: Building Blocks

PROBLEM 1. Visualizing secondary effects in MOS transistors

(a) Plot V_{TH} vs L for both NMOS and PMOS transistors for W = 0.24μm, W = 2μm and W = 10μm.

(b) Plot $V_{GS} - V_{TH}$ vs V_{ov} ($= 2I_{DS}/g_m$) for NMOS and PMOS transistors for W = 0.24μm, W = 2μm and W = 10μm and L = 0.13μm, 0.25μm, 0.36μm, and 0.5μm. Use $V_{DS} = V_{GS}$

(c) Plot g_m vs V_{ov} for NMOS and PMOS transistors for W = 0.24μm, W = 2μm and W = 10μm and L = 0.13μm, 0.25μm, 0.36μm, and 0.5μm. Use $V_{DS} = V_{GS}$

(d) Plot g_m/I_d vs V_{ov} for both NMOS and PMOS transistors for W = 0.24μm, W = 2μm and W = 10μm and L = 0.13μm, 0.25μm, 0.36μm, and 0.5μm.

(e) Plot f_T vs V_{ov} for both NMOS and PMOS transistors for W = 0.24μm, W = 2μm and W = 10μm and L = 0.13μm, 0.25μm, 0.36μm, and 0.5μm.

(f) Plot r_{ds} vs V_{DS} for both NMOS and PMOS transistors for W = 0.24μm, W = 2μm and W = 10μm and L = 0.13μm, 0.25μm, 0.36μm, and 0.5μm. Use $V_{ov} = 0.2$V.

(g) Plot $g_m r_{ds}$ vs V_{DS} for both NMOS and PMOS transistors for W = 0.24μm, W = 2μm and W = 10μm and L = 0.13μm, 0.25μm, 0.36μm, and 0.5μm. Use $V_{ov} = 0.2$V.

PROBLEM 2. Common-source amplifier design

(a) Design a single-stage two-transistor (excluding bias transistors) common-source amplifier with a DC gain of $A_v = 50$V/V, unity gain bandwidth of 200MHz, and an output swing of 400mV (amplitude) with minimum power. Assume supply voltage of 1.3V and a load capacitance of 10pF.

(b) Plot the AC response and clearly indicate the gain and unity gain bandwidth.

(c) Plot A_v vs output DC voltage to illustrate your amplifier achieves $A_v = 50V/V$ over the whole output swing range.

PROBLEM 3. Source follower design

(a) Design a single-stage two-transistor (excluding bias transistors) source follower that level shifts-up the input by 0.8V with a DC gain of $A_v > 0.9$V/V and -3dB bandwidth of 2GHz with minimum power. Assume supply voltage of 1.3V and a load capacitance of 10pF.

(b) Plot the AC response and clearly indicate the gain and unity gain bandwidth.

(c) Plot the step response (use 500mV step input) and determine the settling time.

(d) Calculate the input capacitance and compare it with simulated value.