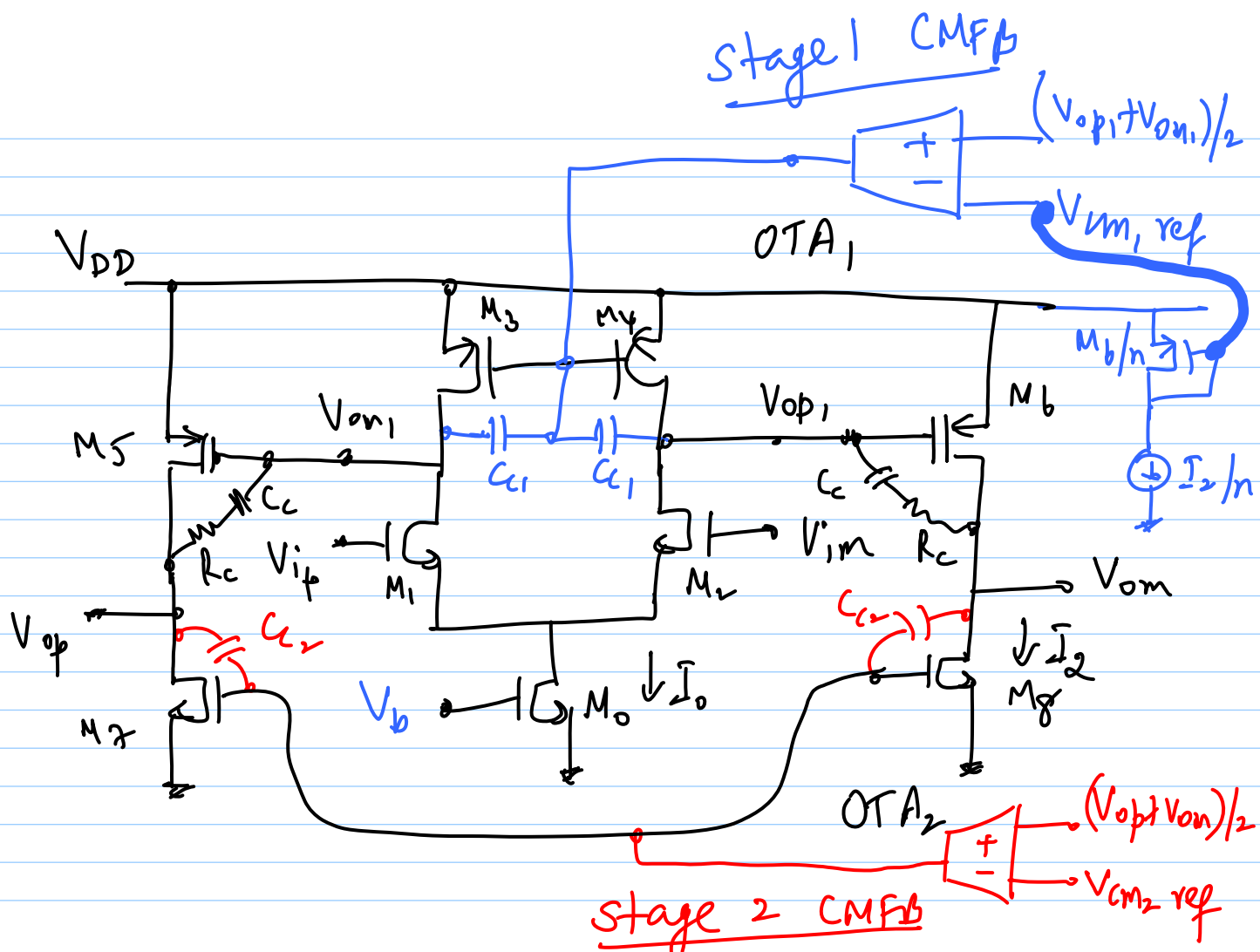


Lec 37

* $V_{0cm_2} \leftarrow$ control gates of M_7/M_8
or gates of M_3/M_4

or gate of M_0
 M_5/M_6 - pseudo diff. pairs
 4 have CM gain



$$* V_{cm,ref} = V_{DD} - V_{SA5} | I_2$$

$$* V_{cm2,ref} = V_{DD}/2 \quad \text{for max swing}$$

Separate CMFB

Stage 1

* Control gates of M₃₄

$$* \text{Set } (V_{op1} + V_{on1})/2 = V_{DD} - V_{SA5} | I_2 = V_{cm,ref}$$

* V_{ref} CM detector which is non-resistive

Stage 2

$$* \quad V_{cm, ref} = V_{DD}/2$$

* resistive CM detection

Common

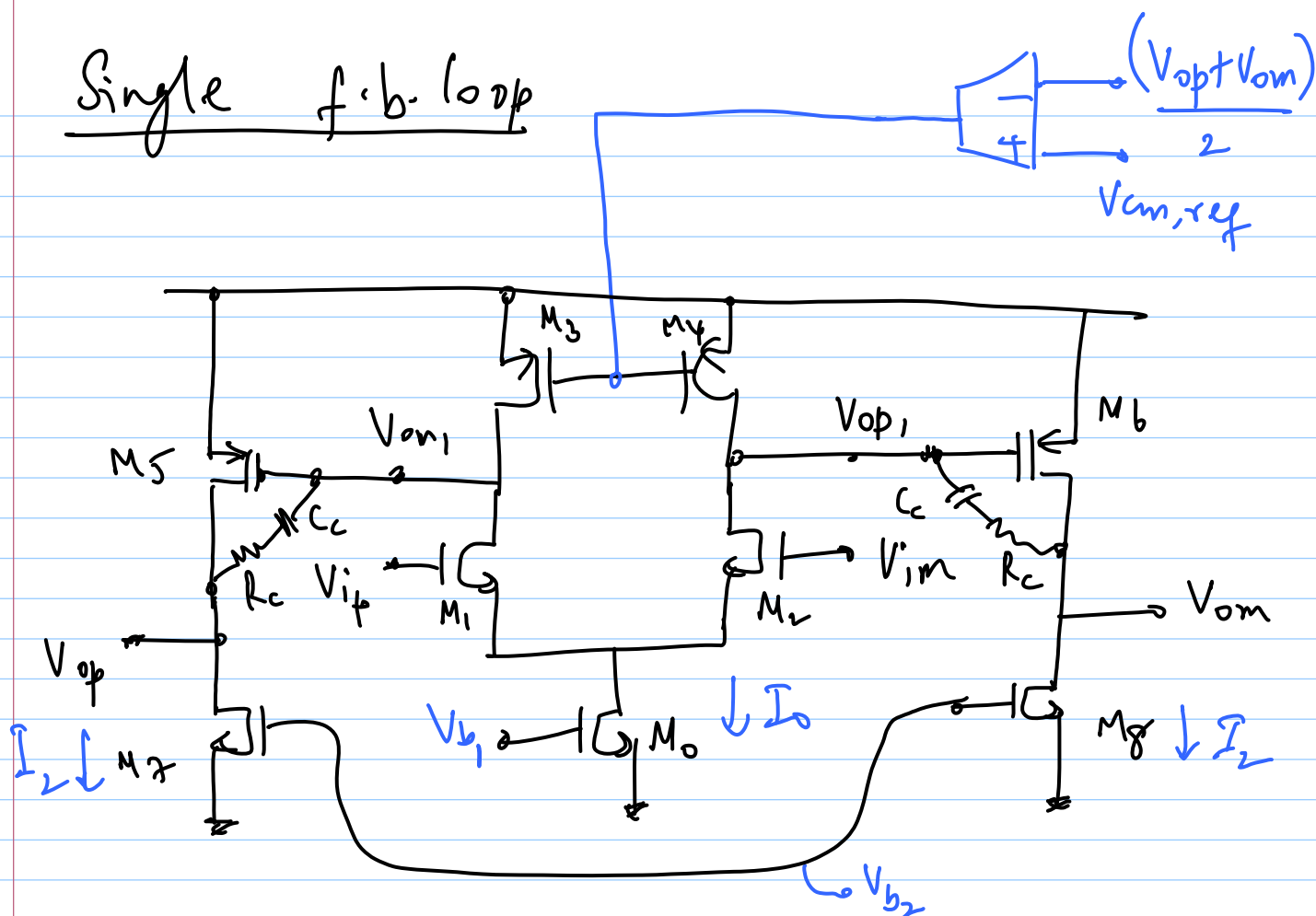
- * Compensation

* V_{IC} 1-stage opamps in CMFB 1 & 2

* OTA₁ - nmos input pair w/ pmos load

OTA₂ - pmos input pair w/ nmos load

Single f.b. loop



Single f.b. loop

- * 3 stages in feedback, lots of gain $\Rightarrow$ harder to stabilise
- * Reduce OTA gain
 - use diode connected loads
- * C_c - can be designed to stabilise CMFB loop as well.