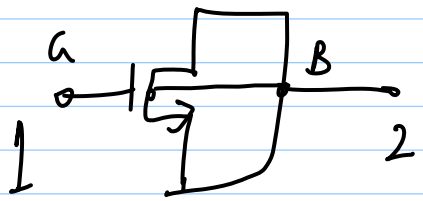
16-1-13

# Lec2

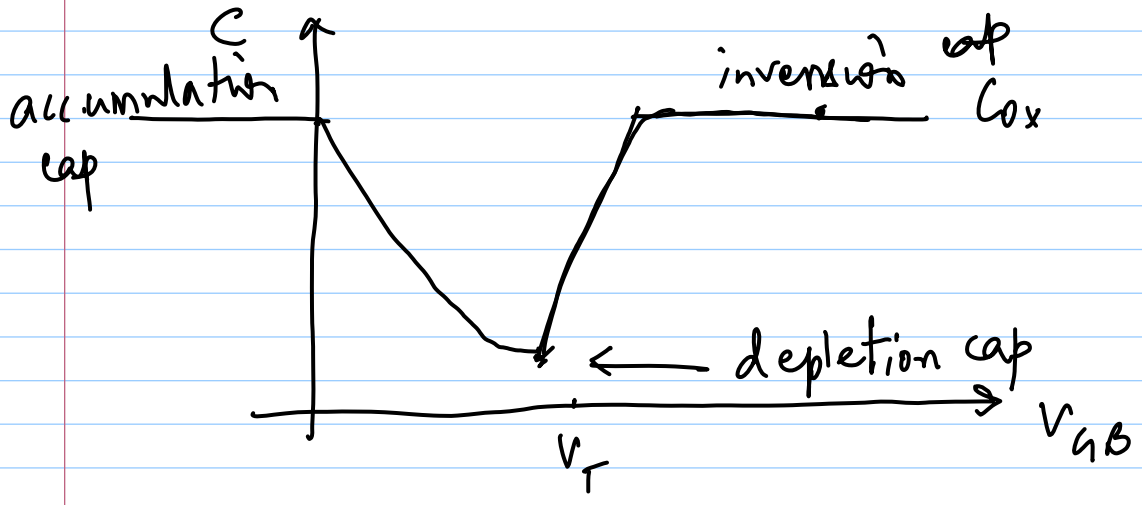
## Capacitor

1)

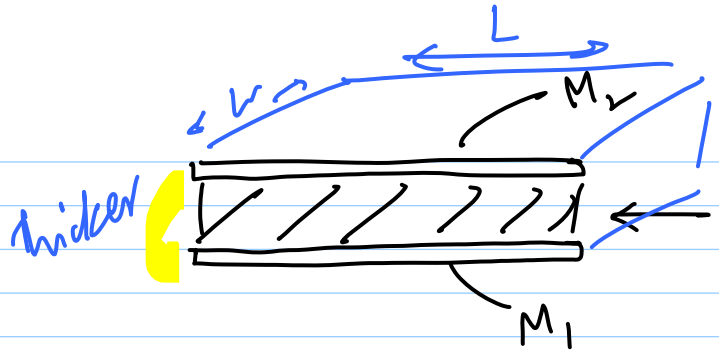



cap between A & inversion layer

if $V_{AB} > V_T$



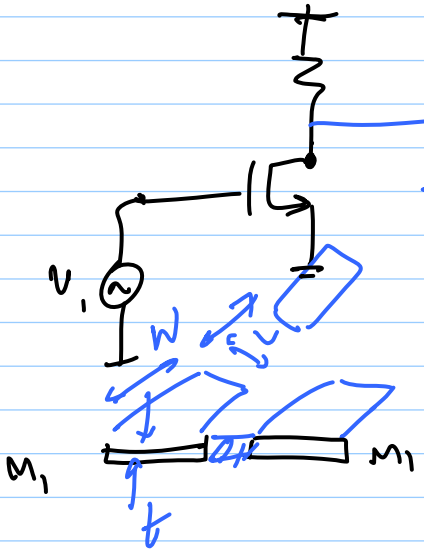

2)




linear

voltage independent

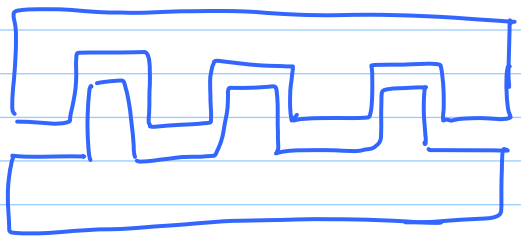
lower density



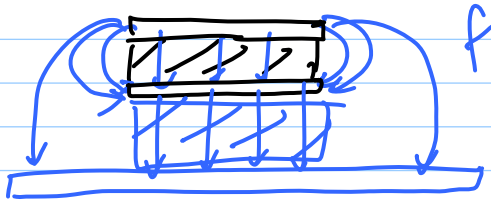

a) Stacking

b) high-k

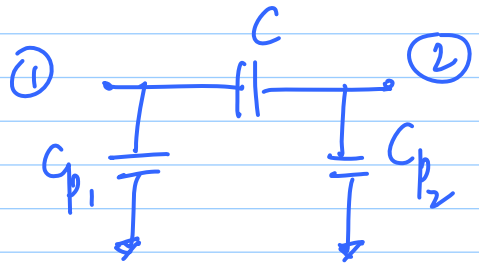
c) horizontal cap



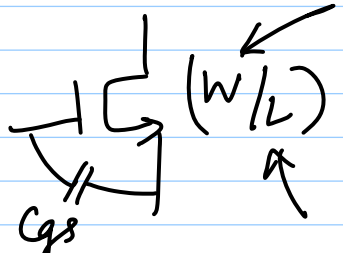

Comb structures
⇒ ↑ density



fringe cap.




Process node — 0.25μm, 0.18μm, 0.13μm ...




$L_{min.} = 0.25\mu m$

$$C_{gs} = \frac{2}{3} W.L.C_{ox}$$ (in sat. region)

Process Scaling

1) Constant Field Scaling
   a) scale lateral & vertical dimensions by $\alpha$ ($>1$)
   b) reduce $V_{DD}$ & $V_T$ by $\alpha$

c) Increase all doping levels by $\alpha$

(I) current $I_D$

$$I_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)(V_{GS}-V_T)^2$$

$$V_{DD} \to \frac{V_{DD}}{\alpha}, \quad V_T \to \frac{V_T}{\alpha}$$

$$V_{GS} \sim \frac{V_{GS}}{\alpha}$$

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \Rightarrow C_{ox}' = C_{ox}\cdot\alpha$$

$$W' = W/\alpha, \quad L' = L/\alpha$$

$$I_D' = \frac{1}{2}\mu_n(\alpha C_{ox})\cdot\frac{(W/\alpha)}{(L/\alpha)}\left(\frac{V_{GS}}{\alpha}-\frac{V_T}{\alpha}\right)^2$$

$$= \frac{1}{\alpha} I_D$$

Capacitance, Power consumption, $g_m$, gate delay, layout density, $f_T$

$$\omega_T \simeq \frac{g_m}{C_{gs}}$$ freq. @ which $\frac{i_{out}}{i_{in}} = 1$

$\omega_{max}$ => freq. @ which power gain = 1