EE5390 Analog Integrated Circuit Design
Assignment 6
Friday 19/04/2013

0.18 μm technology parameters: $V_{Tn} = 0.5$ V; $V_{Tp} = 0.5$ V; $K_n = 300\ \mu A/V^2$; $K_p = 75\ \mu A/V^2$; $A_{VT} = 3.5\, mV\ \mu$m; $A_\beta = 0$; $V_{dd} = 1.8$ V; $L_{min} = 0.18\ \mu$m, $W_{min} = 0.24\ \mu$m; Ignore body effect unless mentioned otherwise.
For all MOS transistors, use $A_d = A_s = 2WL_{min}$; and $P_d = P_s = 2(W + 2L_{min})$ in simulations.

1. **Fully differential two stage opamp design:** The fully differential opamp (Fig. 1 on the last page) should be used to make an amplifier of gain 2 and a closed loop -3 dB bandwidth of $f_b = 5$ MHz with R_L and C_L given below. The phase margin of all loops should be 60°. Minimize the value of miller capacitors in all loops. Use zero cancelling resistors in series with miller capacitors.

Roll no.	input pair	C_L (pF)	R_L (kΩ)
4N	pMOS	10	2.5
4N+1	pMOS	5	5
4N+2	nMOS	10	2.5
4N+3	nMOS	5	5

Tabulate the following:

(a) W, L and operating points (g_m, g_{ds}, V_{GS}-V_T, I_D) of all transistors. Use transistor names given in Fig. 1).

(b) Values of other components in the opamp.

(c) DC gain of the opamp.

(d) DC loop gain of the two common mode feedback loops.

(e) Input referred offset (For this, ignore current factor mismatch; Calculate σ_{VT} from the sizes, and use g_m values from the operating point; You can assume $g_m \gg g_{ds}$).

(f) Power consumption.

Plot the following: (choose appropriate axes limits and font sizes for plotting. Illegible plots do not get any credit).

(a) Differential loop gain-magnitude and phase; Indicate the phase margin.

(b) Differential closed loop gain-magnitude and phase; Indicate the -3 dB bandwidth.

(c) First stage common mode loop gain-magnitude and phase; Indicate the phase margin.

(d) Second stage common mode loop gain-magnitude and phase; Indicate the phase margin.

(e) Transient response of the unity gain inverting amplifier with a 0.2 V differential step (use 0.1 ns rise/fall times).

(f) Transient response of the unity gain inverting amplifier with a 0.1 V common mode step (use 0.1 ns rise/fall times).

(g) Input referred noise spectral density-identify 1/f noise corner. Show relative contributions from different devices at 10 MHz.

Do not use an ideal current sources in the tail. You can use one ideal reference current source of 1/10$^{\text{th}}$ the tail current of the input differential pair for bias generation. Design the bias generator block that generates bias currents and voltages required in the opamp.

Try to determine as many parameters as possible from the specifications and choose sensible starting

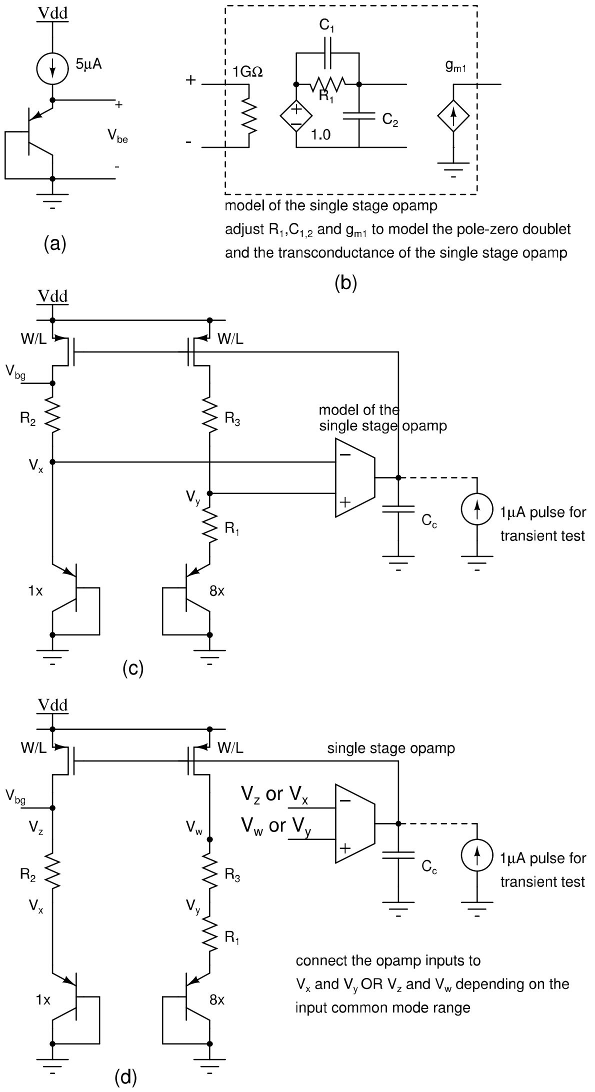

Figure 2: Bandgap reference

points for the others. You can assume a gate overdrive of 200 mV in your initial calculations. Make sure to use replicas correctly (i.e. same transistor length) wherever applicable.

2. **Bandgap reference**: Bias a 1x sized diode connected PNP[1] at 5 μA as shown in Fig. 2(a) and sweep the temperature from 0 to 100°C. Determine dV_{BE}/dT at 27°C.

   Design the bandgap shown in Fig. 2(c). Choose R_1 for a quiescent current of 5 μA and R_2 to get zero temperature coefficient at V_{bg}. Choose $R_3 = R_2$. What is the role of R_3? Simulate the bandgap reference with the model of a single stage opamp assuming that the single stage opamp is made like the first stage of the previous problem. (Fig. 2(b)-model the gm, and the pole zero doublet). Choose C_c for ringing $\leq 10\%$. Test the bandgap reference by sweeping the temperature from 0 to 100°C and plot V_{bg}. Test the transient response by applying a 1 uA pulse to the output of the opamp. Adjust the values of R_1, R_2, $R_3 (= R_2)$ if necessary to get zero TC at 27°C.

   Modify the circuit as in Fig. 2(d). How should V_x, V_y, and V_{bg} change? What is the purpose of this modification? Resimulate with the opamp model as before and test the temperature sensitivity, transient response and the loop gain.

   Substitute the differential pair opamp designed in the previous assignment and simulate the temperature sensitivity of V_{bg} and the transient response to a current step at the output.

[1]Use the model `ideal_pnp` in `ideal_diode.lib`

The following two problems need not be submitted. You may do them for improving your understanding.

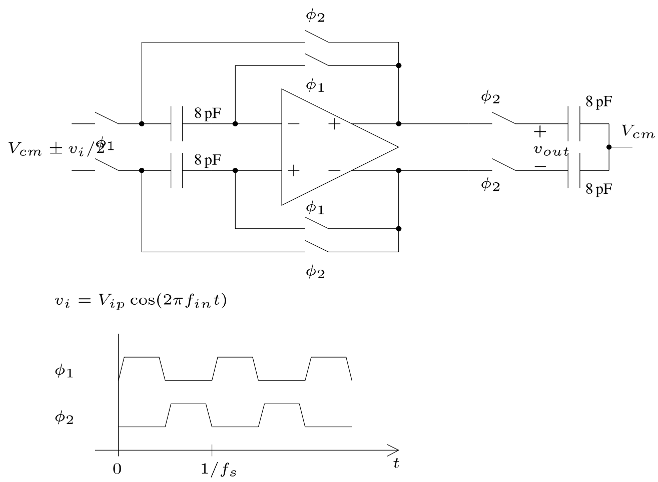

Figure 3: Sample and hold circuit

1. **Sample and hold**: Design the sample and hold circuit in Fig. 3 using the fully differential folded cascode opamp designed above. Use ideal switches with 1 kΩ on resistance. Use $f_s = 4$ MHz and $f_{in} =$

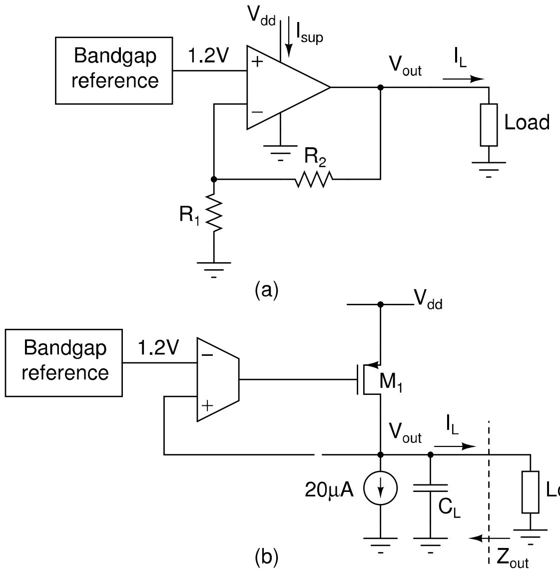

Figure 4: Low dropout regulator

$\{1/4, 9/4\}$ MHz (sinusoidal input with 1.6 Vppd[2] amplitude) and plot the output waveforms. Provide a plot that shows the settling behavior of the opamp.

2. **Low dropout regulator (LDO)**: A voltager regulator is nothing but a noninverting amplifier whose input is the bandgap voltage from a reference. In Fig. 4(a), the output voltage is $(R_2/R_1)V_{bg}$. By making R_2 variable, one can get a variable voltage output.

    - The output impedance should be very low: This is accomplished by realizing a very high loop gain over as wide a bandwidth as possible.
    - The efficiency $((V_{out}I_L)/(V_{dd}I_{sup}))$ should be very high: For this, the current $I_{sup} - IL$ consumed by the circuit should be minimized (This makes it hard to satisfy the previous condition). The "dropout" $V_{dd} - Vout$ should be minimized.
    - Usually only a positive I_L needs to be driven. The output voltage is constant over time. These are departures from conventional amplifiers.

    Fig. 4(b) shows a "pass transistor" M_1 enclosed in a feedback loop. For simplicity, a unity gain case is shown. M_1 should have a high enough W/L to remain in saturation with the desired dropout and the highest output current. Miller compensation around M_1 is usually not used because it severely compromises power supply rejection (Incremental voltage gain from V_{dd} to the output voltage).

    Use the model in Fig. 2(b) for the single stage opamp. Use a 50 μA quiescent current in M_1. Adjust the width (with minimum length) of M_1 for a dropout of 300 mV with a 50 mA current. You can use a 1.2V voltage source in place of the bandgap reference. Compensate the loop using a load capacitor C_L for a phase margin of 45° at $I_L = 0$ and $I_L = 50$ mA and choose the higher one. Do the following (except the last one) for two cases ($I_L = 0$ and $I_L = 50$ mA—you can use a current source for the load):

    (a) Vary V_{dd} from 1.4 V to 1.8 V and plot V_{out}

    (b) Plot Z_{out} from 1 kHz to 10 MHz

    (c) Plot the transfer function from V_{dd} to V_{out} from 1 kHz to 10 MHz

    (d) Plot the small signal step response for a 10 μA step in the output current

    (e) Plot the large signal step response (I_L switching from zero to 50 mA and 50 mA to zero)

[2] Vppd: volts, peak-peak differential

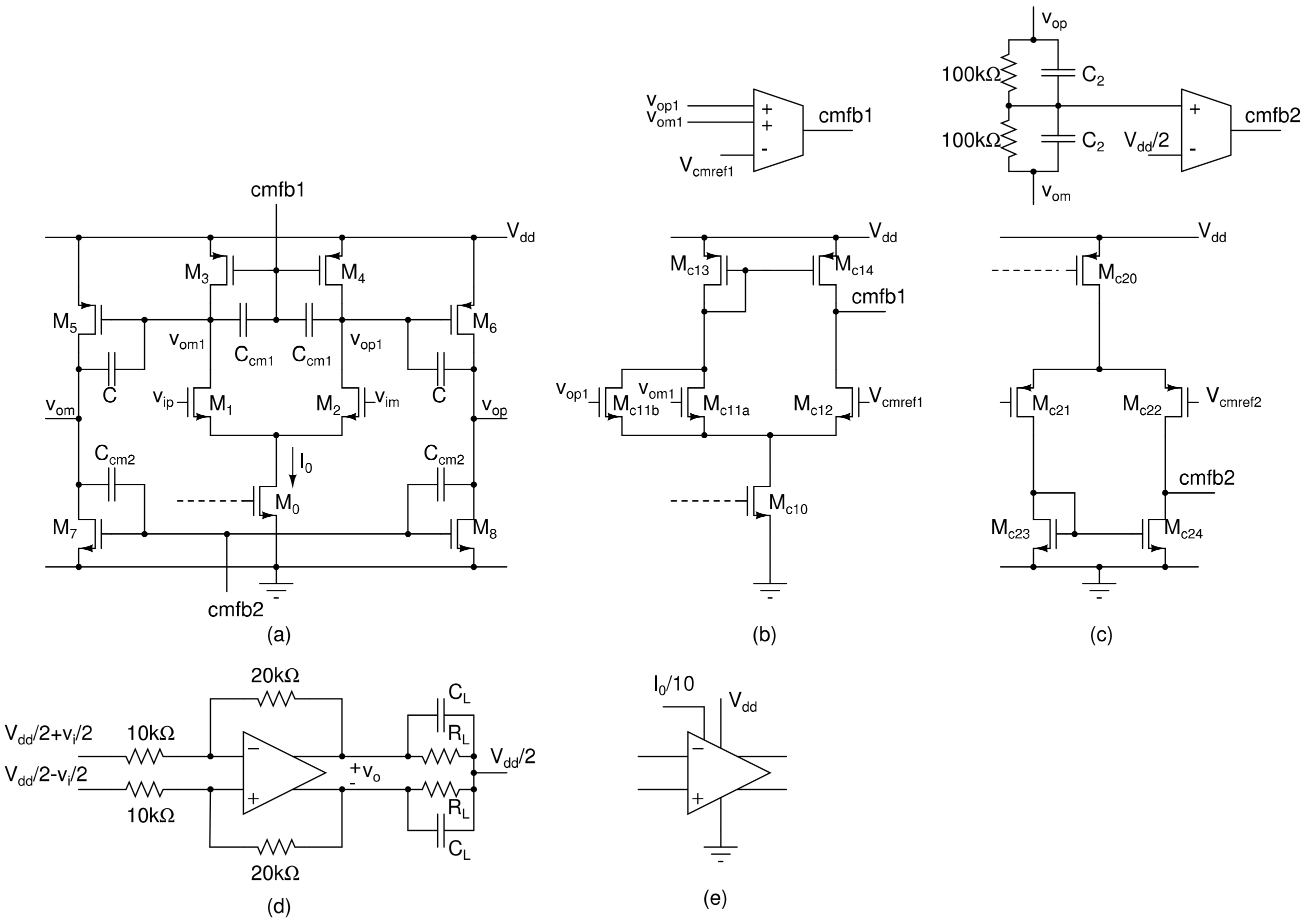

Figure 1: (a) Fully differential two stage opamp (Zero cancelling resistors not shown), (b) First stage common mode feedback, (b) Second stage common mode feedback, (d) Closed loop amplifier, (e) External connections to the opamp. *With a pMOS input pair, all transistors will be of the opposite polarity*