EE5390: Analog Integrated Circuit Design

Project 1

due on 8 April 2012 11:59 pm

Fully differential two stage opamp design

Use $A_{V_T} = 3.5mV - \mu m$; $A_\beta = 0$; $W_{min} = 0.25\mu m$; Slew rate = $5V/\mu s$. Ignore body effect unless mentioned otherwise.

The fully differential opamp (Fig. 1 on the last page) should be used to make an amplifier of gain 2 and a closed loop -3 dB bandwidth of $f_b = 5MHz$ with R_L and C_L given below. The phase margin of all loops should be 60^o. Minimize the value of miller capacitors in all loops. Use zero cancelling resistors in series with miller capacitors.

Roll no.	input pair	$C_L(pF)$	$R_L(k\Omega)$
4N	pMOS	10	2.5
4N+1	pMOS	5	5
4N+2	nMOS	10	2.5
4N+3	nMOS	5	5

Tabulate the following:

1. W, L and operating points ($g_m, g_{ds}, V_{GS} - V_T, I_D$) of all transistors. Use transistor names given in Fig. 1.
2. Values of other components in the opamp.
3. DC gain of the opamp.
4. DC loop gain of the two common mode feedback (CMFB) loops.
5. Input referred offset (For this, ignore current factor mismatch; Calculate σ_{V_T} from the sizes, and use g_m values from the operating point; You can assume $g_m >> g_{ds}$).
6. Power consumption.

Plot the following: (choose appropriate axes limits and font sizes for plotting. Illegible plots do not get any credit).

1. Differential loop gain - magnitude and phase; Indicate the phase margin.
2. Differential closed loop gain - magnitude and phase. Indicate the -3 dB bandwidth.
3. First stage common mode loop gain - magnitude and phase; Indicate the phase margin.
4. Second stage common mode loop gain - magnitude and phase; Indicate the phase margin.
5. Trasient response of the unity gain inverting amplifier with a 0.2 V differential step (use 0.1 ns rise/fall times).

6. Trasient response of the unity gain inverting amplifier with a 0.1 V common mode step (use 0.1 ns rise/fall times).

7. Slew Rate should be simulated and plotted for both positive and negative steps. Input for the closed-loop amplifier should be stepped from a) 0 to VDD and b) VDD to 0.

8. Input referred noise spectral density - identify 1/f noise corner. Show relative contributions from different devices at 10 MHz.

Do not use ideal current sources in the tail. You can use one ideal reference current source of $1/10^{th}$ the tail current of the input differential pair for bias generation. Design the bias generator block that generates bias currents and voltages required in the opamp.

Try to determine as many parameters as possible from the specifications and choose sensible starting points for the others. You can assume a gate over drive of 200 mV in your initial calculations. Make sure to use replicas correctly (i.e., same transistor length) wherever applicable.

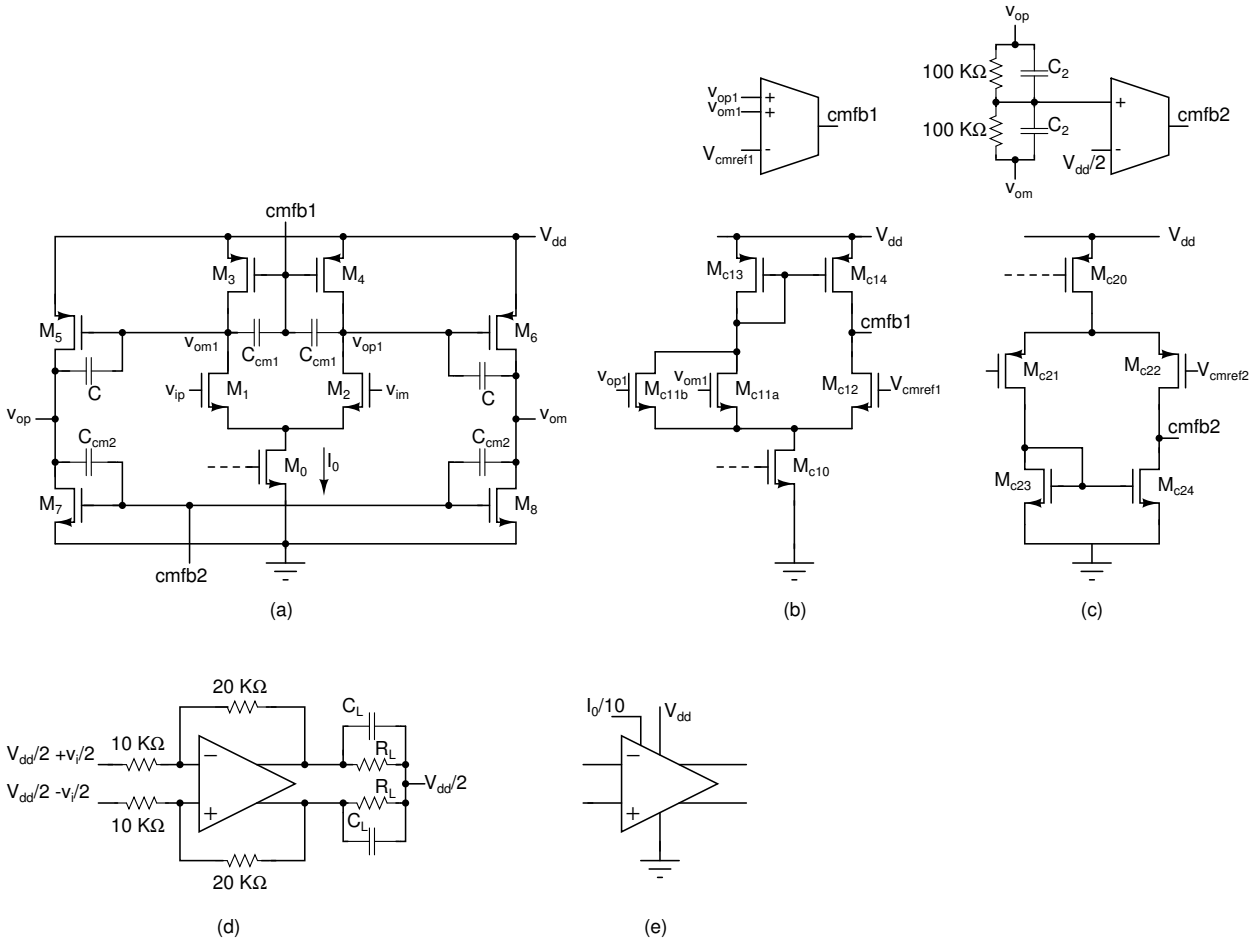

Figure 1: (a) Fully differential two stage opamp (Zero cancelling resistors not shown), (b) First stage common mode feedback, (b) Second stage common mode feedback, (d) Closed loop amplifier, (e) External connections to the opamp.

With a pMOS input pair, all transistors will be of the opposite polarity.