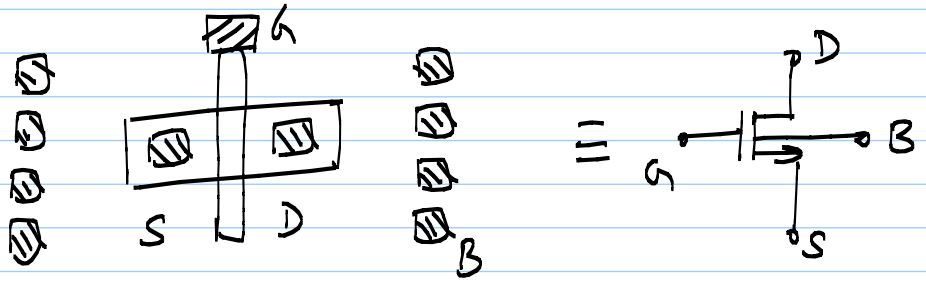
19-4-12

Lec 44

Layout: Geometries that appear on masks used in fabrication ⇒ top view of the devices and associated connections (routings)

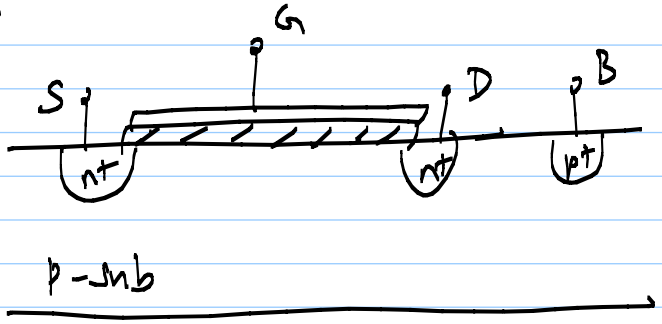
top view of a MOSFET (layout)



reminder: MOSFETs are 4-terminal devices

→ Bulk (substrate) contacts are critical!

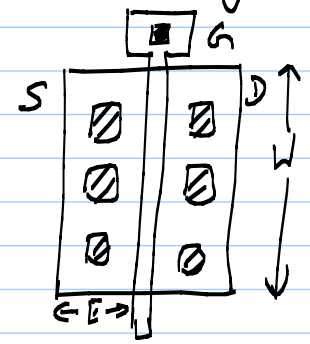
Side view (conceptual):

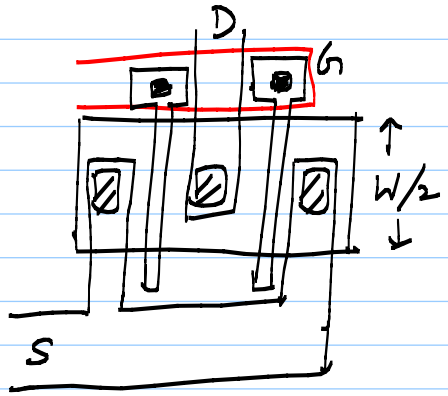


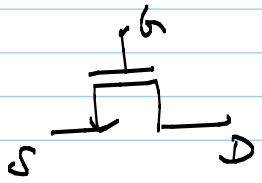
* be aware of noise-sensitive & noise-producing circuits in and around your circuit location
* time: only ~50% time spent in design
  other 50% time – layout
* several iterations are common for sensitive circuits ⇒ increases design cycle time

Analog/RF layout practices

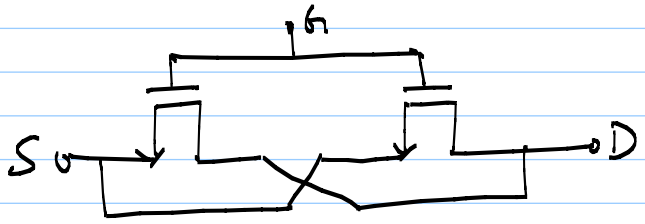
1) Multi finger transistors







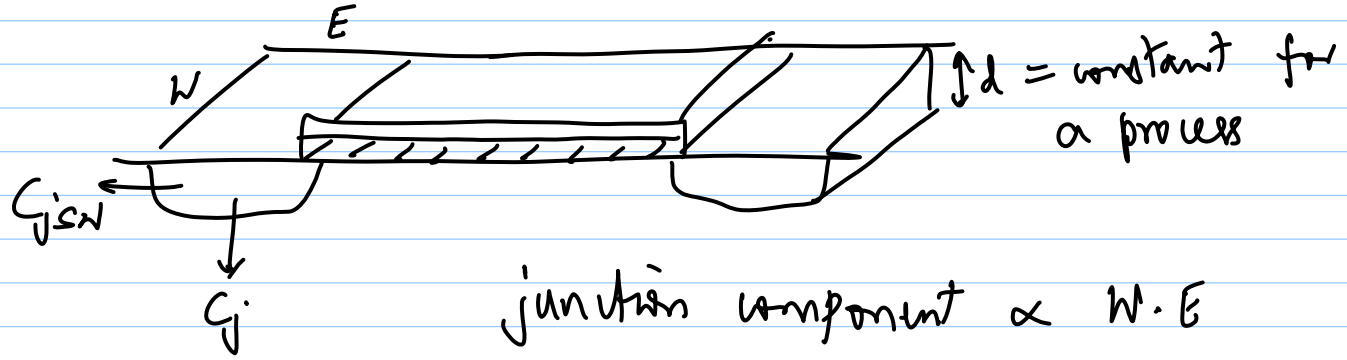
(a)



(b)

S/D Capacitance

C_{DB} & C_{SB} : → junction cap - C_j
→ sidewall cap - C_{jsw}



junction component ∝ W · E

SW component ∝ W

Note: C_j = ____ $fF/\mu m^2$

C_{jsw} = ____ $fF/\mu m$

(a) : $C_{DB_a} = C_{SB_a} = W \cdot E \cdot C_j + 2(W+E)\, C_{jsw}$

(b) : $C_{DB_b} = \frac{W}{2} \cdot E \cdot C_j + 2\left[\frac{W}{2} + E\right] \cdot C_{jsw}$

$$C_{SB_b} = 2\left[\frac{W}{2} \cdot E \cdot C_j + 2\left(\frac{W}{2} + E\right) \cdot C_{jsw}\right]$$

$$= W \cdot E \cdot C_j + 2(W + 2E) \cdot C_{jsw}$$

for same total W/L,

$$C_{DB_b} < C_{DB_a}$$

Gate resistance $= r_g$

poly resistance is usually given in $\Omega/\square$

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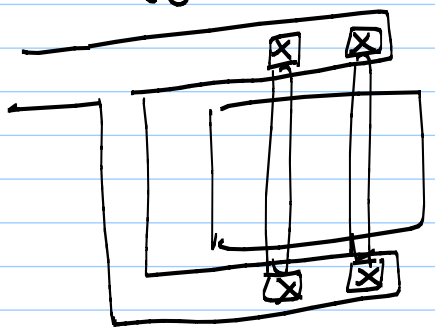
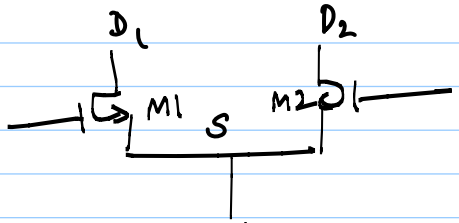
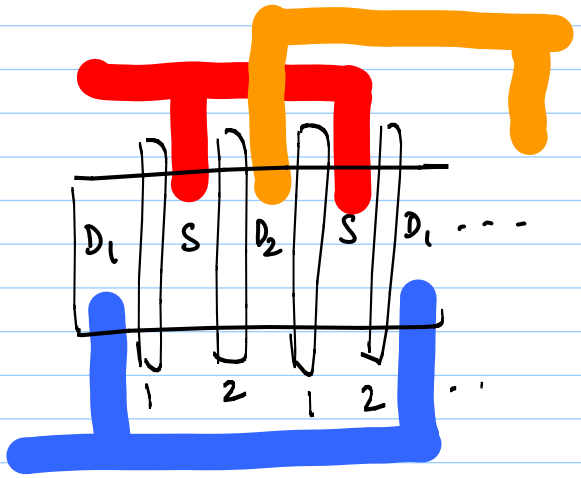
* Try to contact gate from both sides
* r_g can also produce resistive noise
* Do not route gate in poly
  - → between fingers or
  - → in any connection to gate



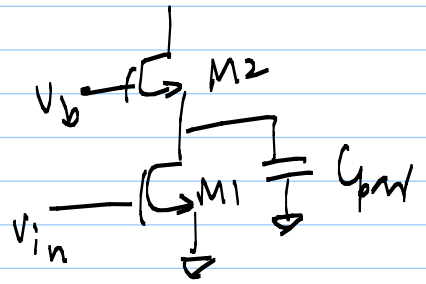
2) Interdigitisation :





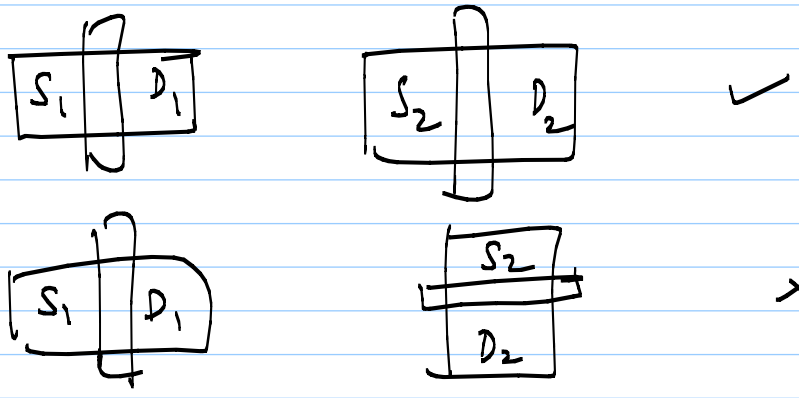
* process related effects are distributed out

* improves matching and symmetry in current mirrors, diff pairs, cascodes etc.
→ reduces CM noise coupling, even order non-linearities

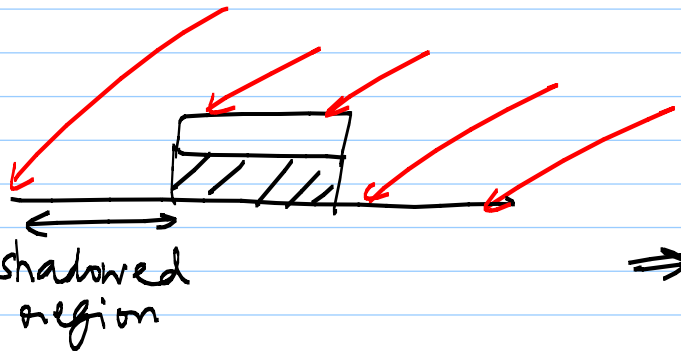


* reduces cap between cs & cascode through shared S-D node
* saves area

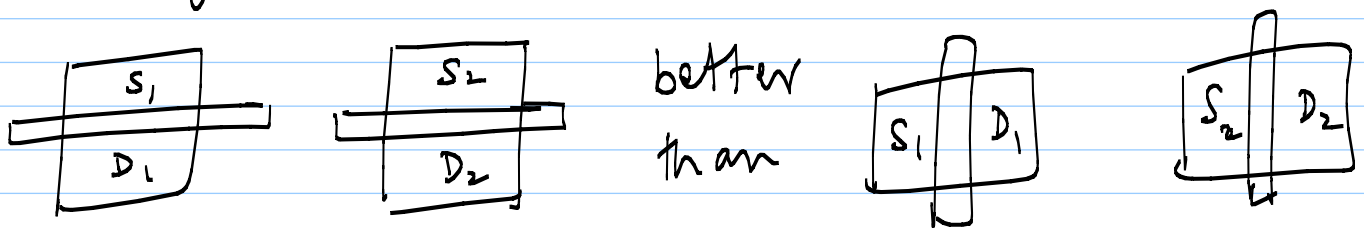
3) <u>other techniques for Symmetry</u> :
→ Intn digitisation is layout-intensive
→ can also add extra R-C parasitics
a) Same orientation – to remove process effects



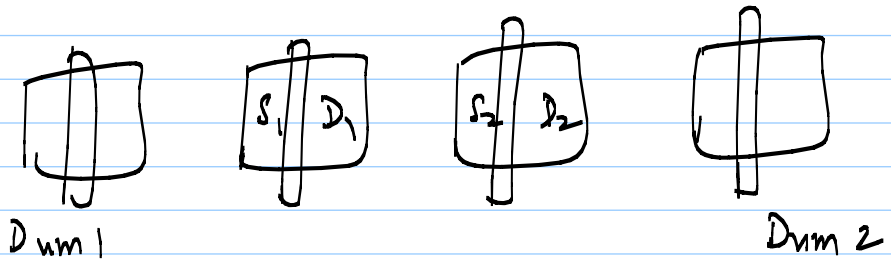
b) Add dummies (takes care of gate-shadowing)

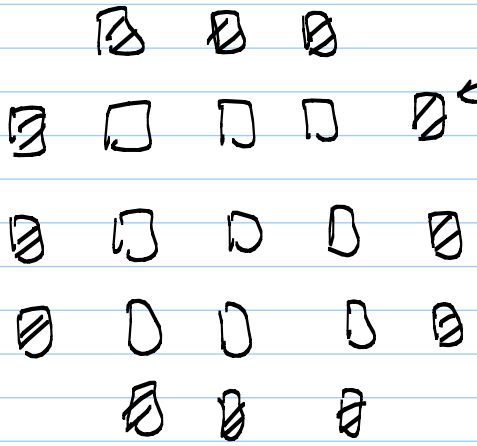


⇒ S-D asymmetry



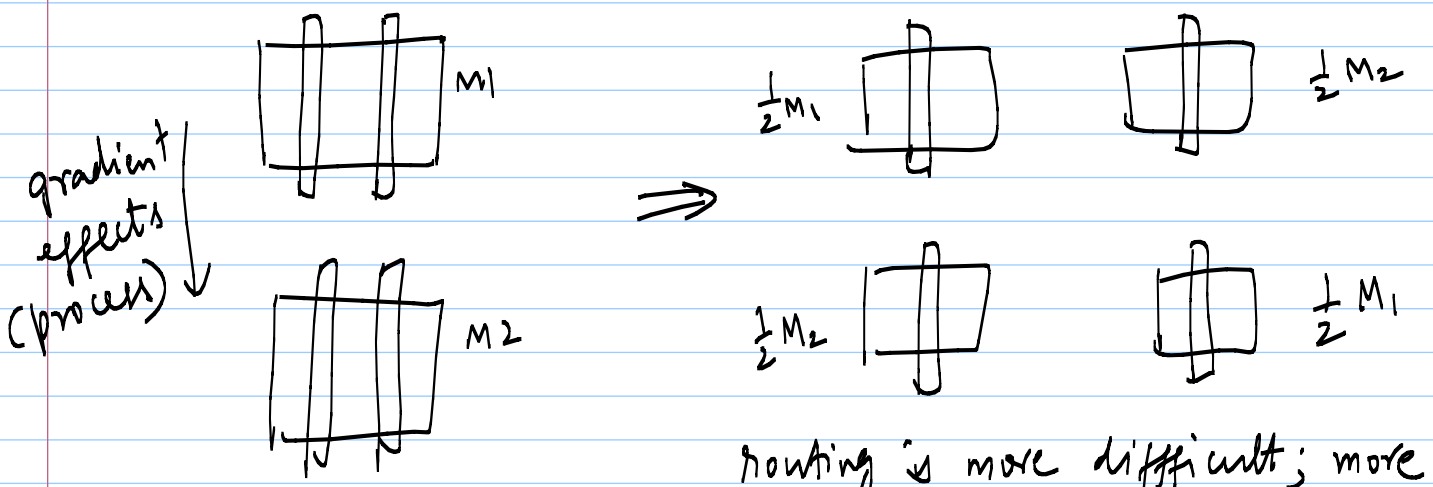
better option — add dummy devices





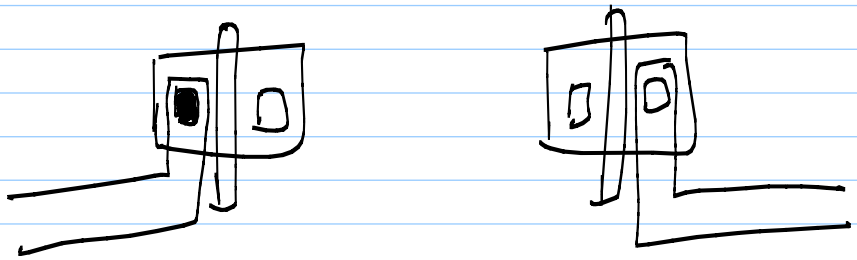
Basic idea: maintain same environment on either axis of symmetry

c) Common centroid:



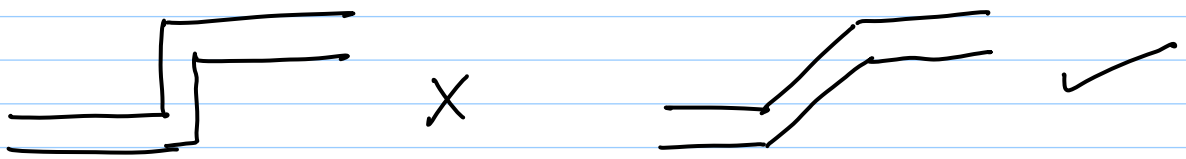
routing is more difficult; more parasitic cap is possible

d) matching environment:



metal lines can affect parasitic cap to device nodes!

e) 45° lines:



→ help with charge crowding at corners

→ improves electromigration effects

f) maintain symmetry in routing (differential)

e.g.