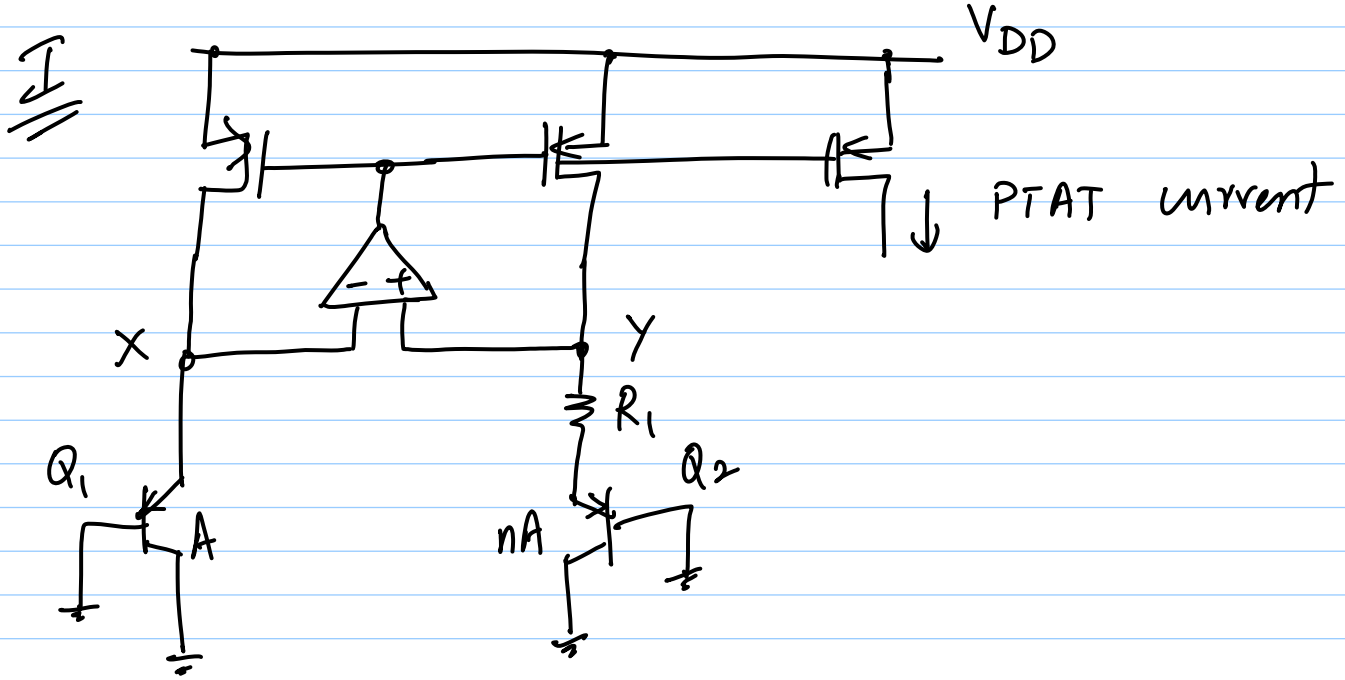
4-4-12

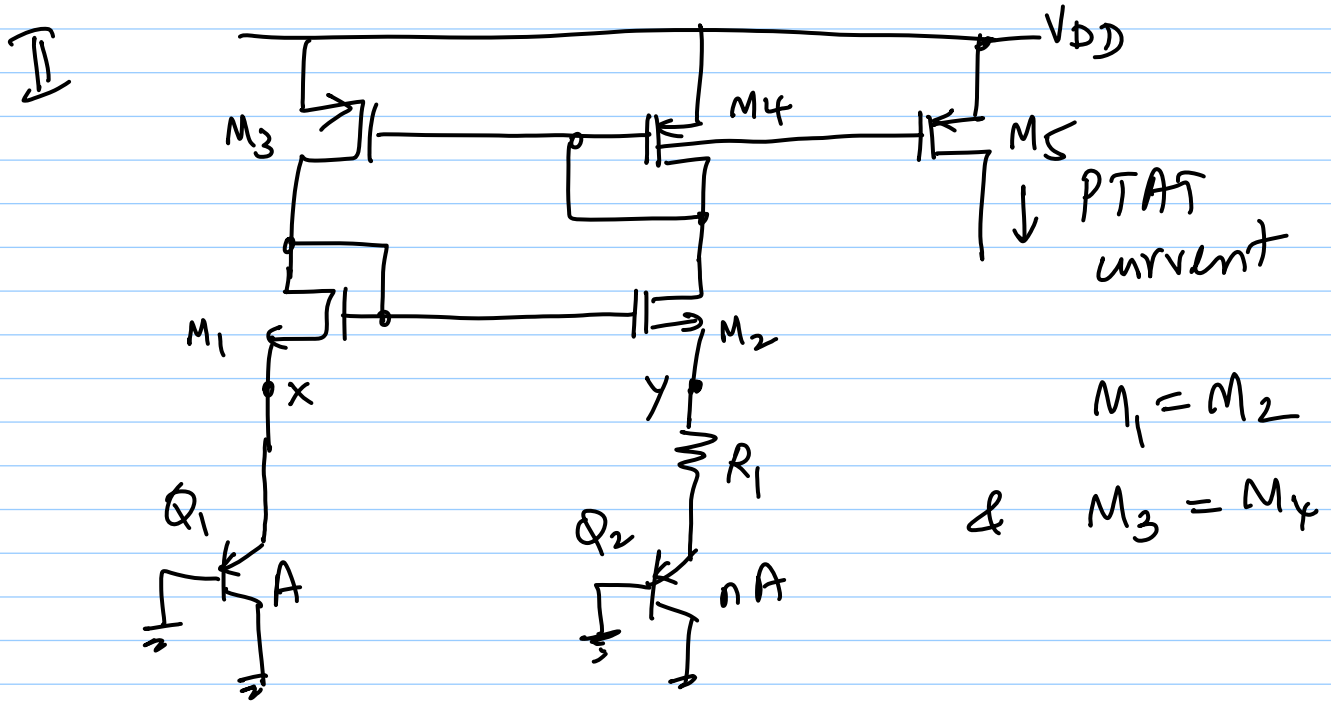
Lec 38

PTAT current

I



II



$M_1 = M_2$ & $M_3 = M_4$

$I_{D_1} = I_{D_2} \Rightarrow V_{GS_1} = V_{GS_2} \Rightarrow V_X = V_Y$

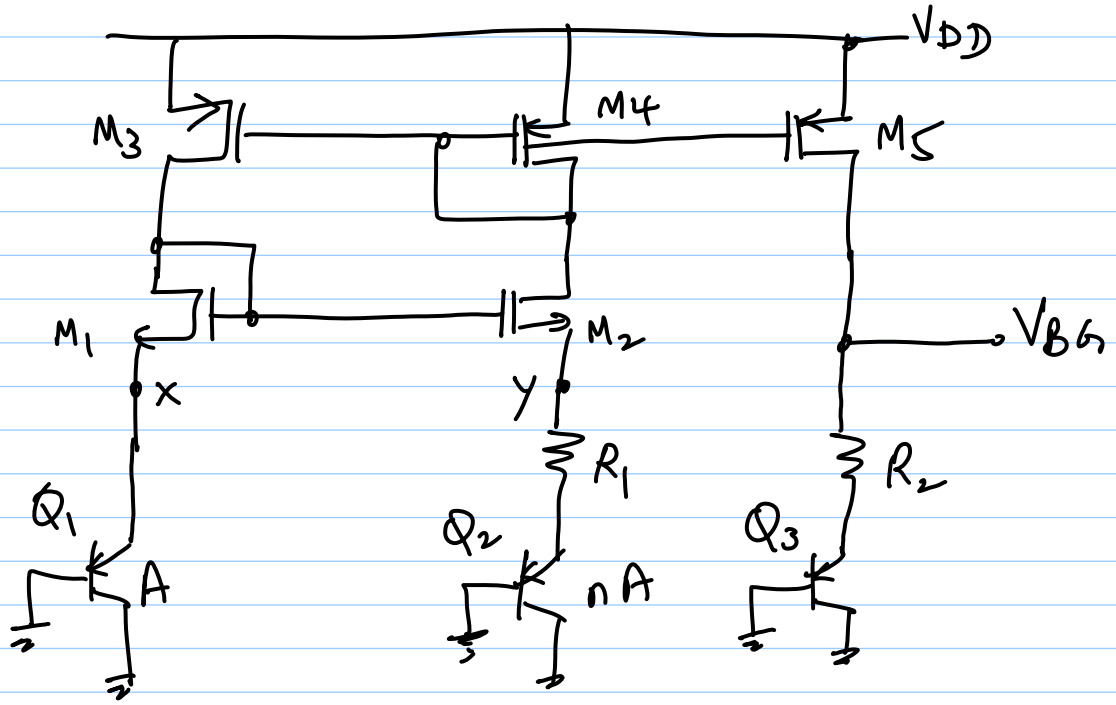
$\Rightarrow I_{D_1} = I_{D_2} = (V_T \ln n)/R_1 \{\propto I_{D_5}\}$

deviations caused by
→ mismatches
→ R_1 tempco

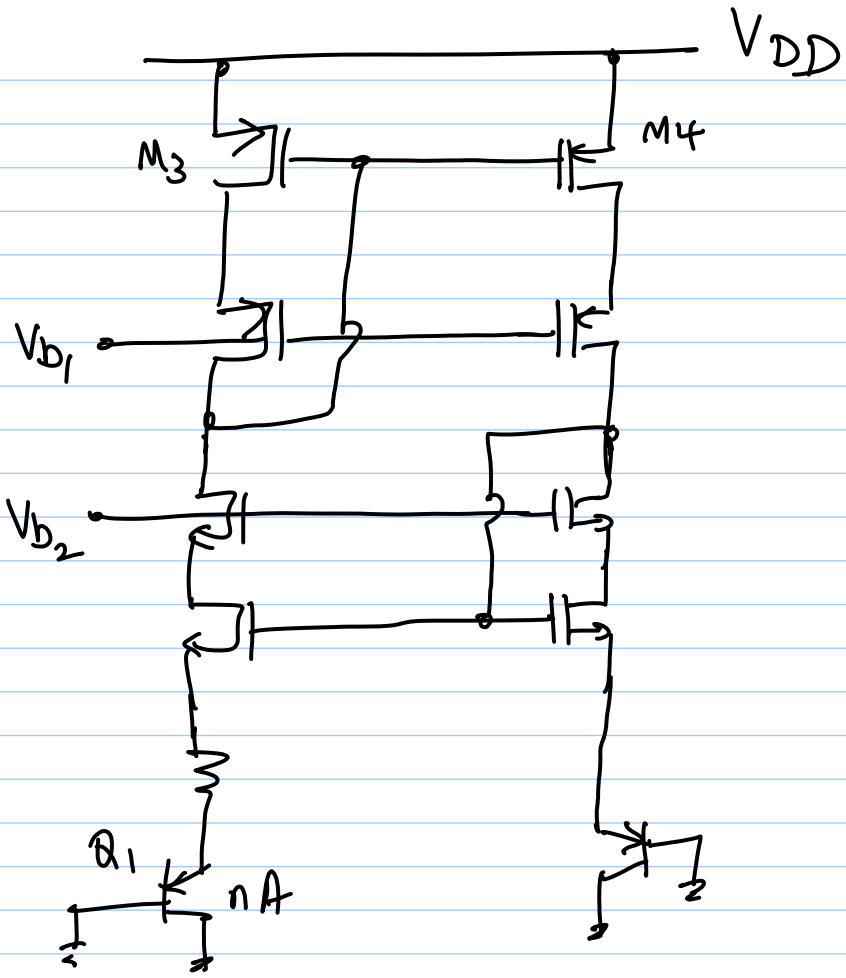
Bandgap from PTAT

$$V_{BG} = \alpha_1 V_{BE} + \alpha_2 V_{PTAT}$$
$$= \alpha_1 V_{BE} + \alpha_2 \cdot R \cdot I_{PTAT}$$

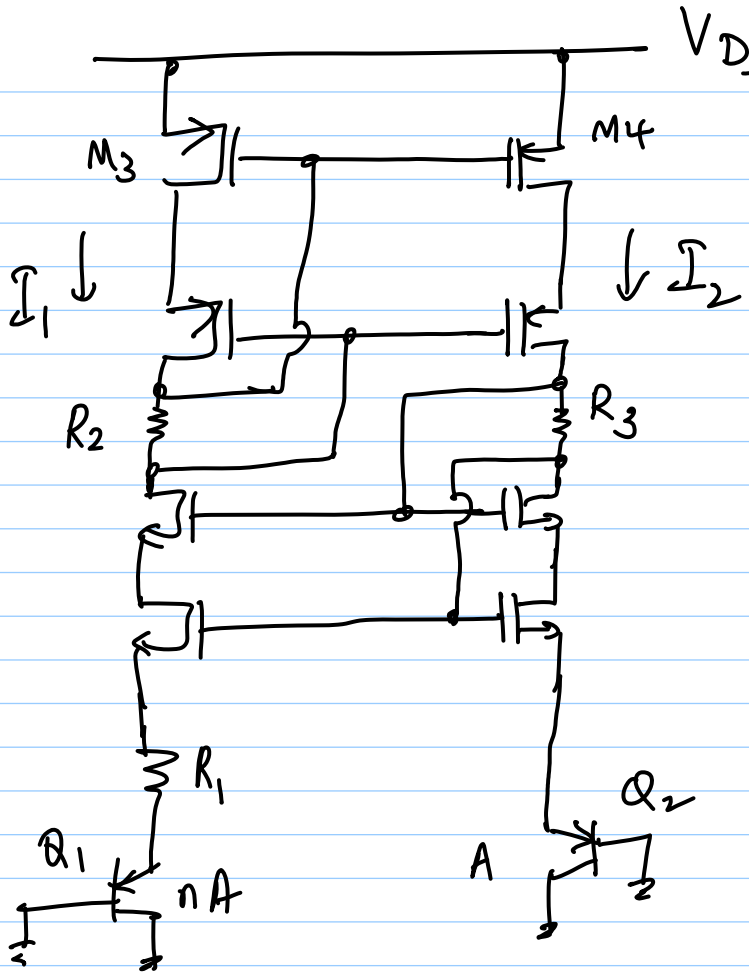
* Reduce supply dependence due to CLM in pmos devices
⇒ Cascode mirrors



$$V_{BG} = V_{BE_3} + \frac{R_2}{R_1} V_T \ln n$$

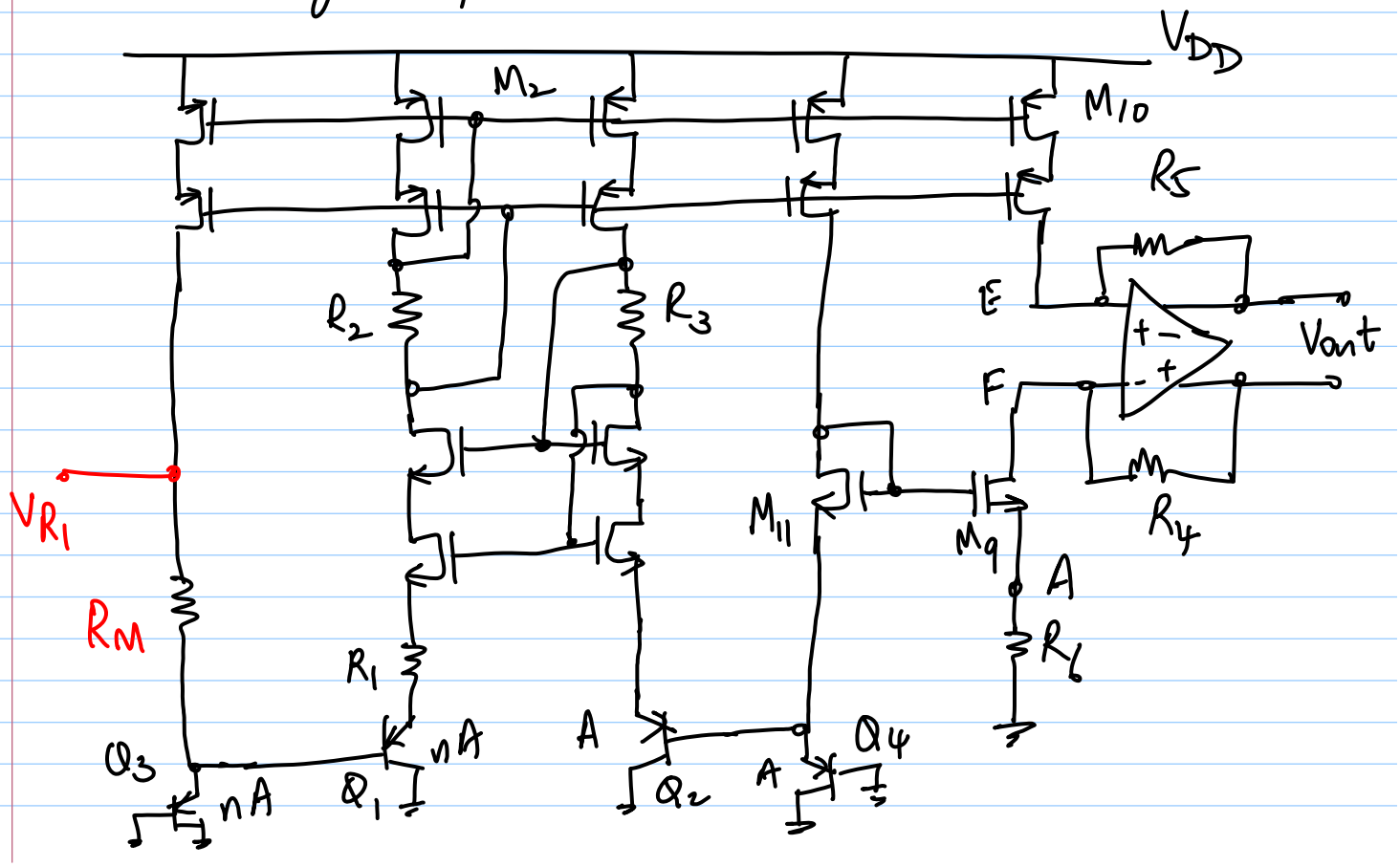


need to generate V_{b_1} & V_{b_2}



self-biased cascodes

Floating reference



* If $M_9 = M_{11}$,

$$V_A = V_{BE_4} + V_{GS_{11}} - V_{GS_9} = V_{BE_4}$$

$$\Rightarrow I_{D_9} = \frac{V_{BE_4}}{R_6} \Rightarrow V_{R_4} = V_{BE_4}\left(\frac{R_4}{R_6}\right)$$

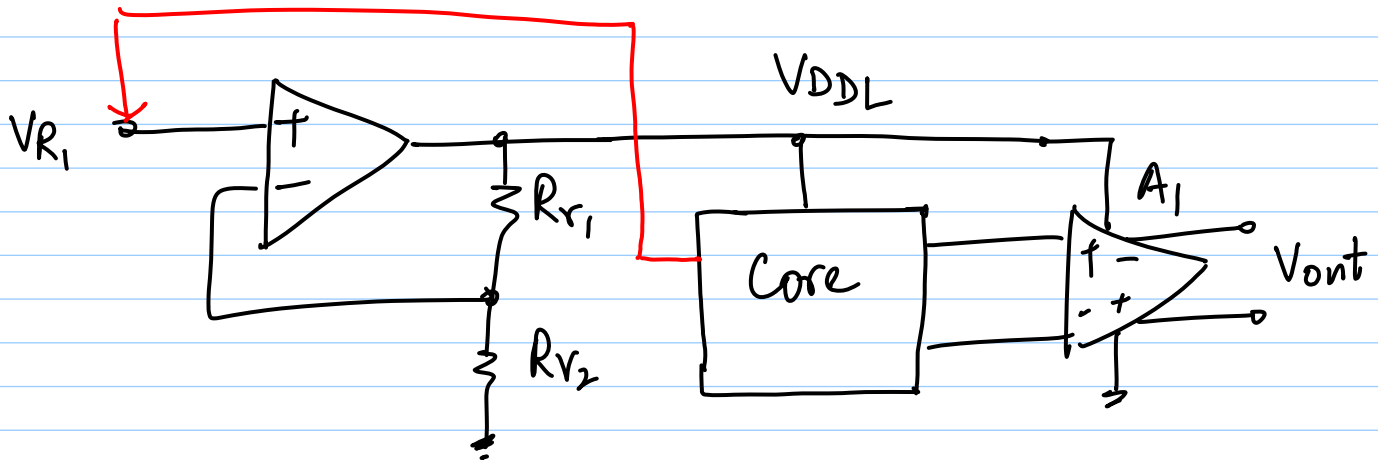
* If $M_{10} = M_2$,

$$I_{D_{10}} = \frac{2(V_T \ln n)}{R_1}$$

$$\Rightarrow V_{R_5} = 2V_T \ln n \left(\frac{R_5}{R_1}\right)$$

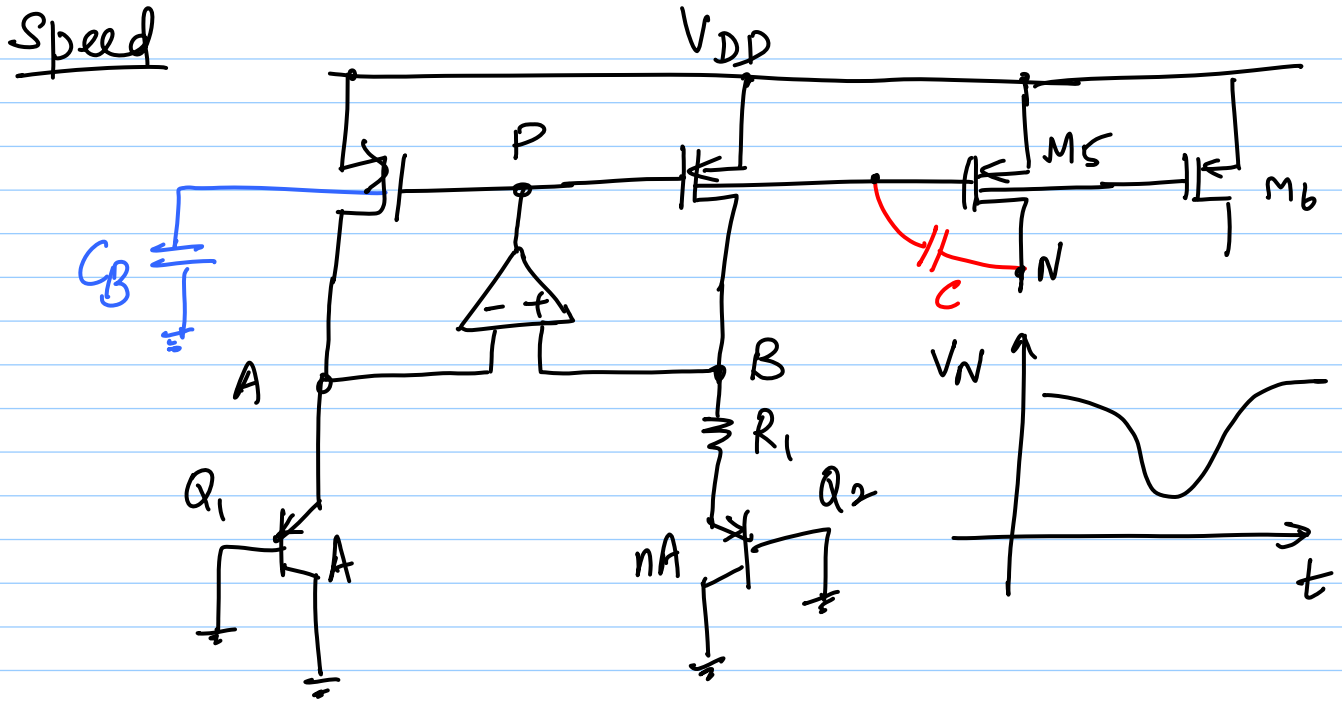
Opamp ensures $V_E = V_F$

$$\Rightarrow \quad V_{out} = \frac{R_4}{R_1} V_{BE_4} + 2\frac{R_3}{R_1} V_T \ln n$$



* improves supply rejection
* V_{R_1} generated from inside core (R_m)
* Requires startup ckt

Speed

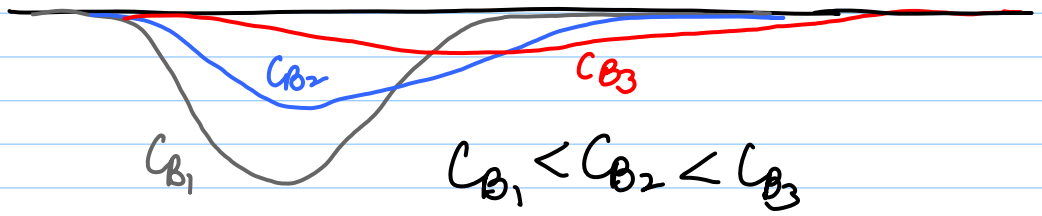


* If V_N changes quickly, V_P cannot follow (opamp) $\Rightarrow$ $I_{D_5} \neq I_{D_6}$ have transients

* V_p may take a long time to settle
  ⇒ high speed opamp required

* Or: add a cap C_B @ P (bypass)
  → opamp stability degrades
    i.e. opamp has to be 1-stage
  → $C_B \gg C$

However: Once disturbed, large settling time



Noise

* Noise in ref directly goes to o/p of any ckt

Here Noise from:

1) Opamp → thermal
   → 1/f
2) Resistors → thermal
3) BJT → shot
   → 1/f
   → thermal (r_B etc.)