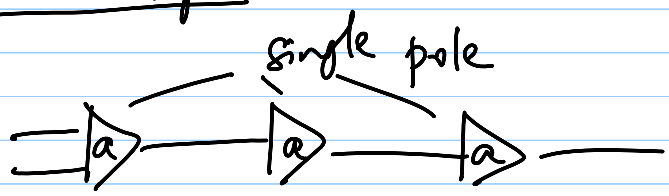
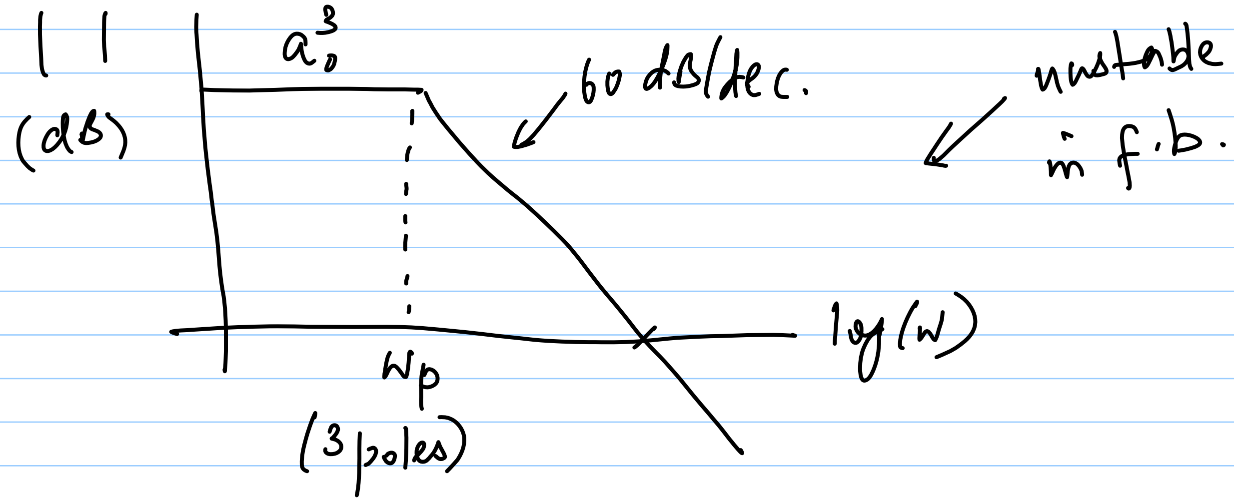
29-3-12

Lec - 35

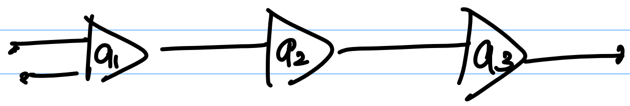
3-stage Opamp

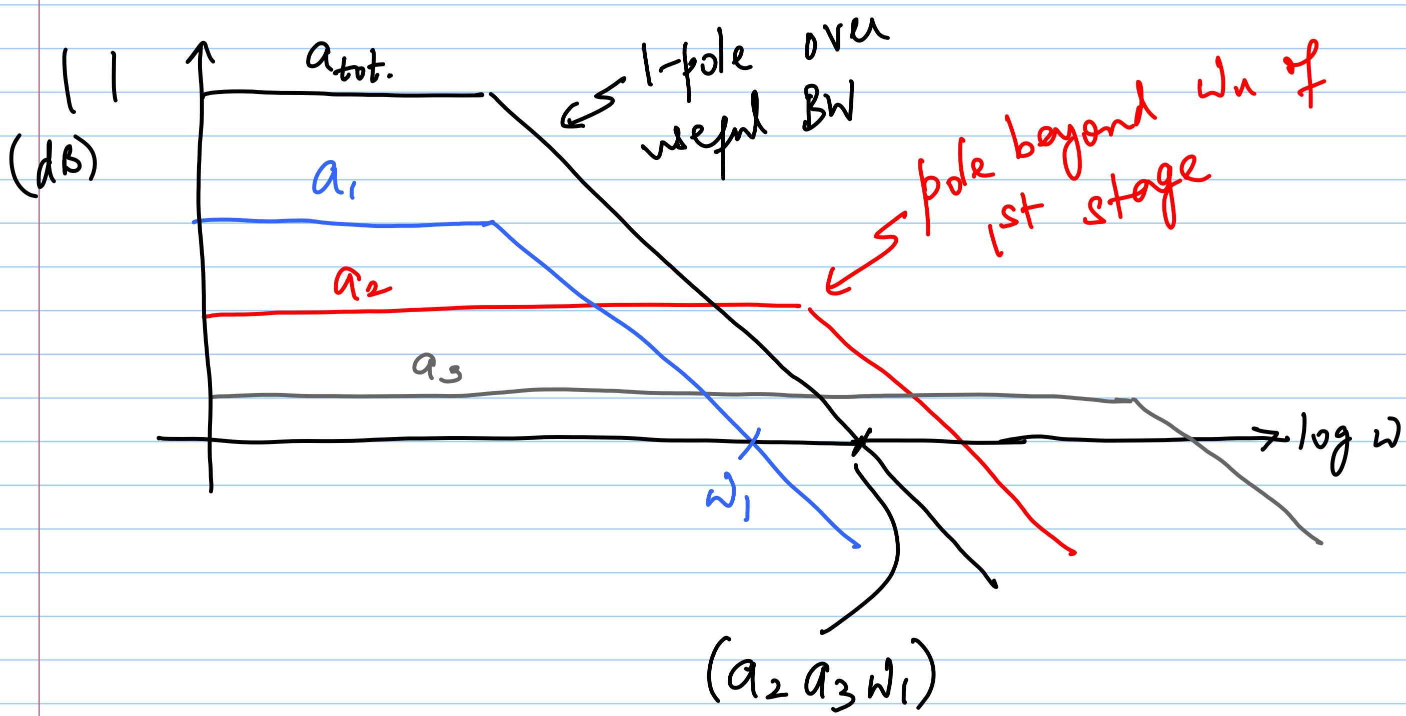
Hacker design

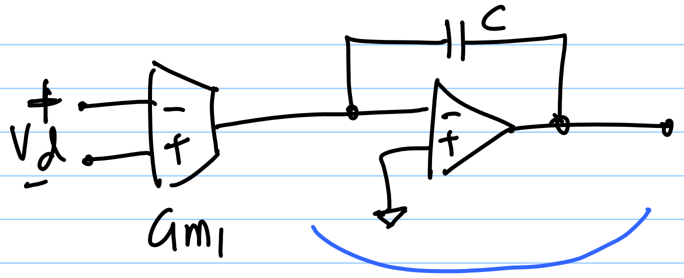




better design: BW of later stages wider





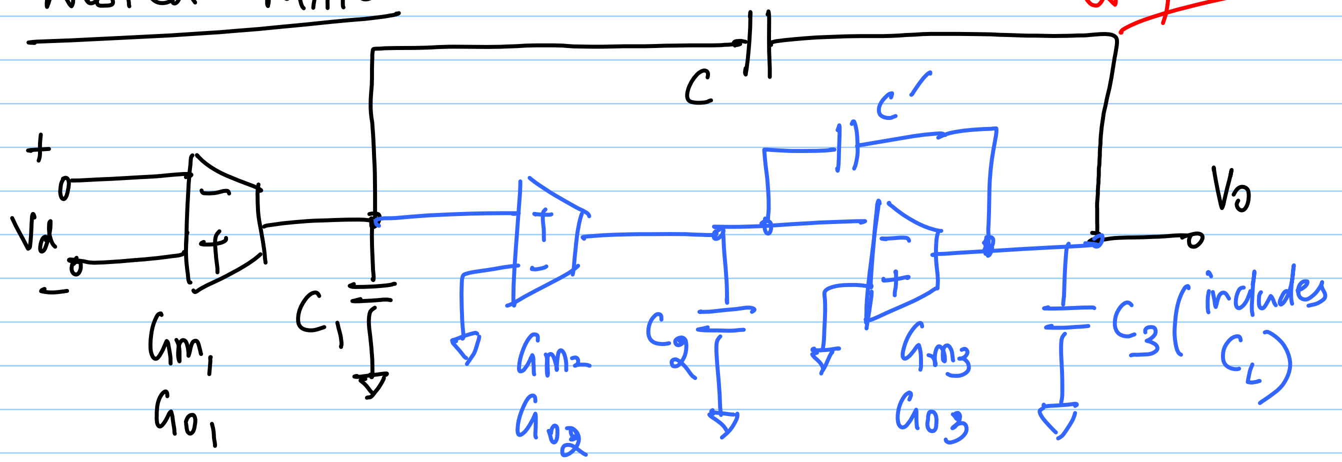


$$V_o = V_d \cdot \frac{G_{m1}}{sC}$$

= 2-stage opamp

Nested miller compensation

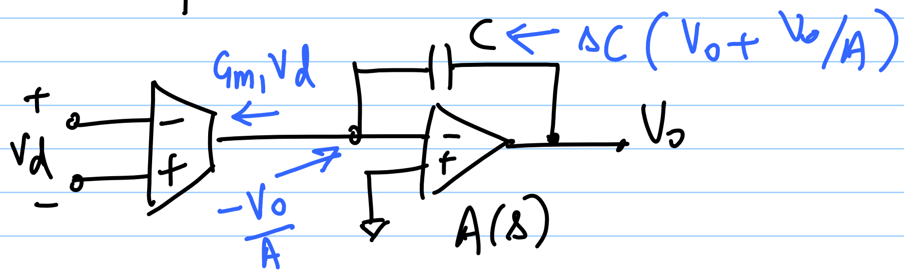
1) Nested Miller



$$\omega_u = \frac{G_{m1}}{C} \quad (\text{desired})$$

dc gain $A_o = \dfrac{G_{m1}\,G_{m2}\,G_{m3}}{G_{o1}\,G_{o2}\,G_{o3}}$ (large)

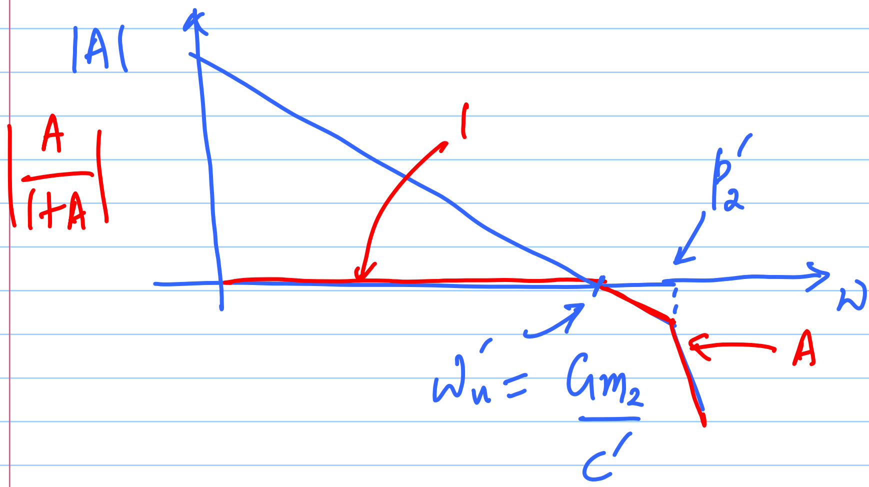
dominant pole $\omega_d \simeq \omega_u / A_o$



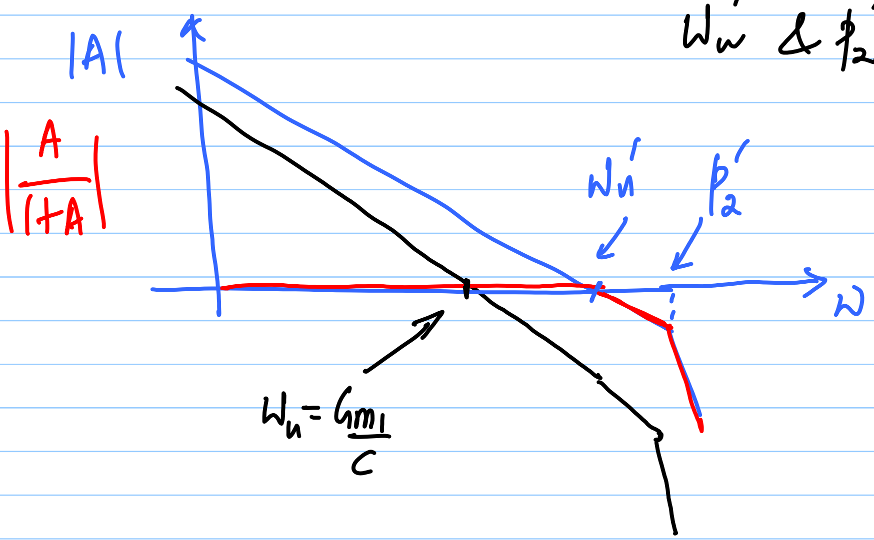
$$G_{m1}V_d \simeq sC\left(V_o + V_o/A\right)$$

neglecting G_{o1} (at hi-freq.)

$$\Rightarrow \quad \frac{V_o}{V_d}(s) = \frac{G_{m1}}{sC}\,\frac{1}{\left(1+\frac{1}{A}\right)} = \frac{G_{m1}}{sC}\cdot\frac{A}{1+A}$$



$$|A| \gg 1 \;\Rightarrow\; \frac{A}{1+A} \approx 1 \;;\; |A| \ll 1 \Rightarrow \frac{A}{1+A} \approx A$$



ω_u' & $p_2' \gg \frac{G_{m1}}{C}$ (2 non-dominant poles)

* Non-dominant poles & zeroes of A appear as they are in $A/(1+A)$
* There will be a pole of $A/(1+A)$ at UGF of A

Conditions

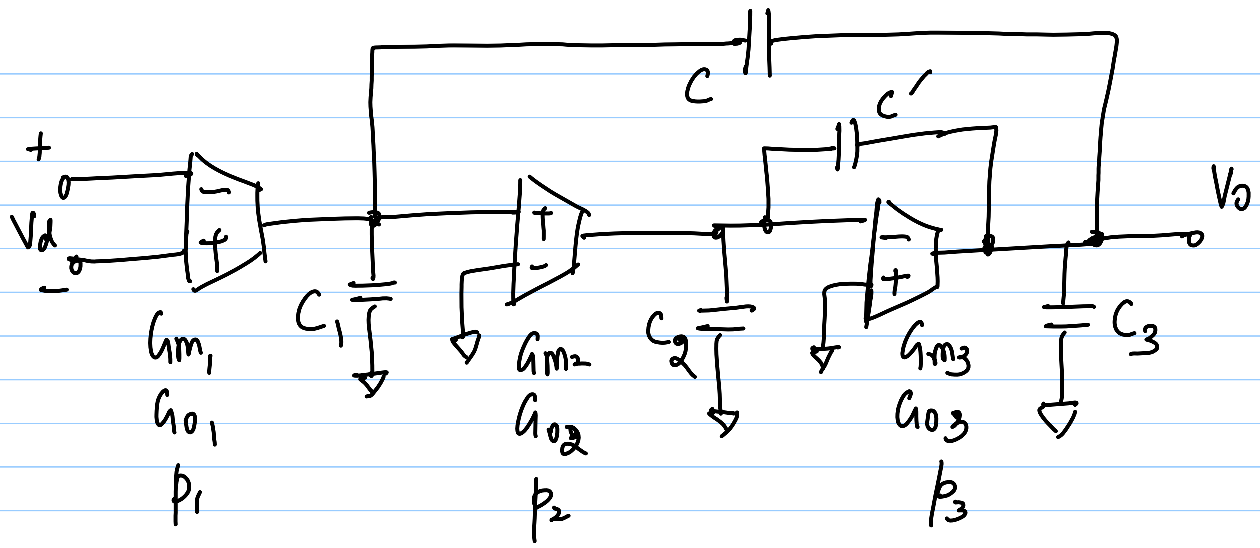
* $$\frac{G_{m1}}{C} < \omega_u' < p_2' = \frac{G_{m2}\frac{C'}{C'+C_2}}{\frac{C'C_2}{C'+C_2}+C_3}$$

$$\omega_u' \; \left(\frac{G_{m2}}{C'}\right)$$

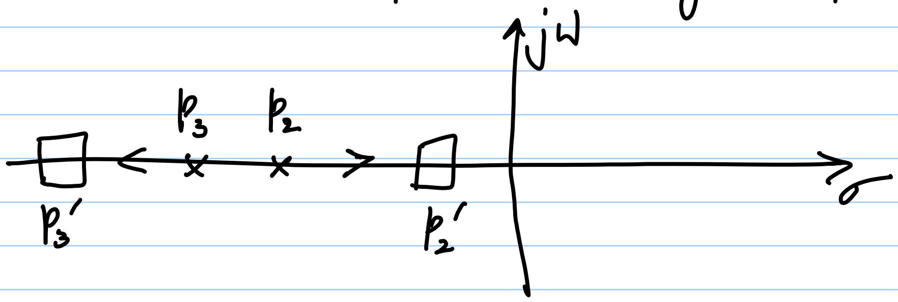
→ 3-stage opamps will be slower than 2-stage opamps

→ steady state error will be very smaller

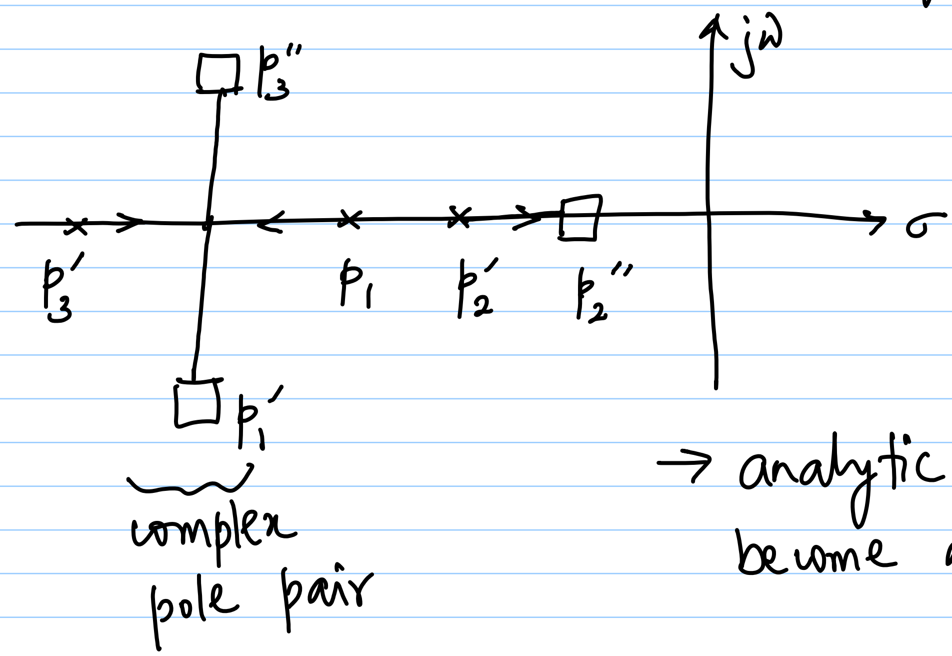
* This analysis assumes inner opamp is ideal VCVS (zero positions are inaccurate)



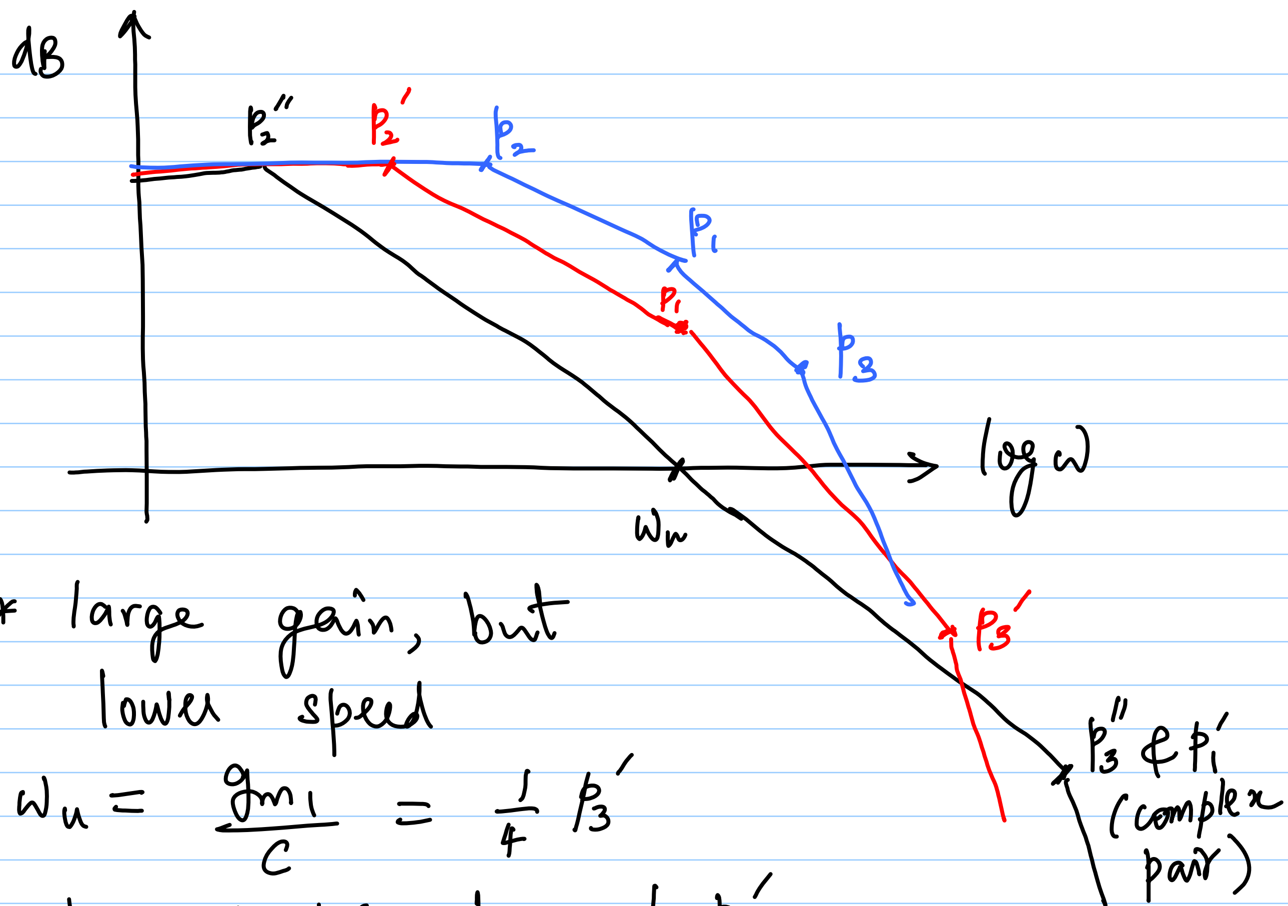
* add C' ⇒ p_3 & p_2 get split



* add C $\Rightarrow$ Second splitting



$\rightarrow$ analytic design can become quite difficult



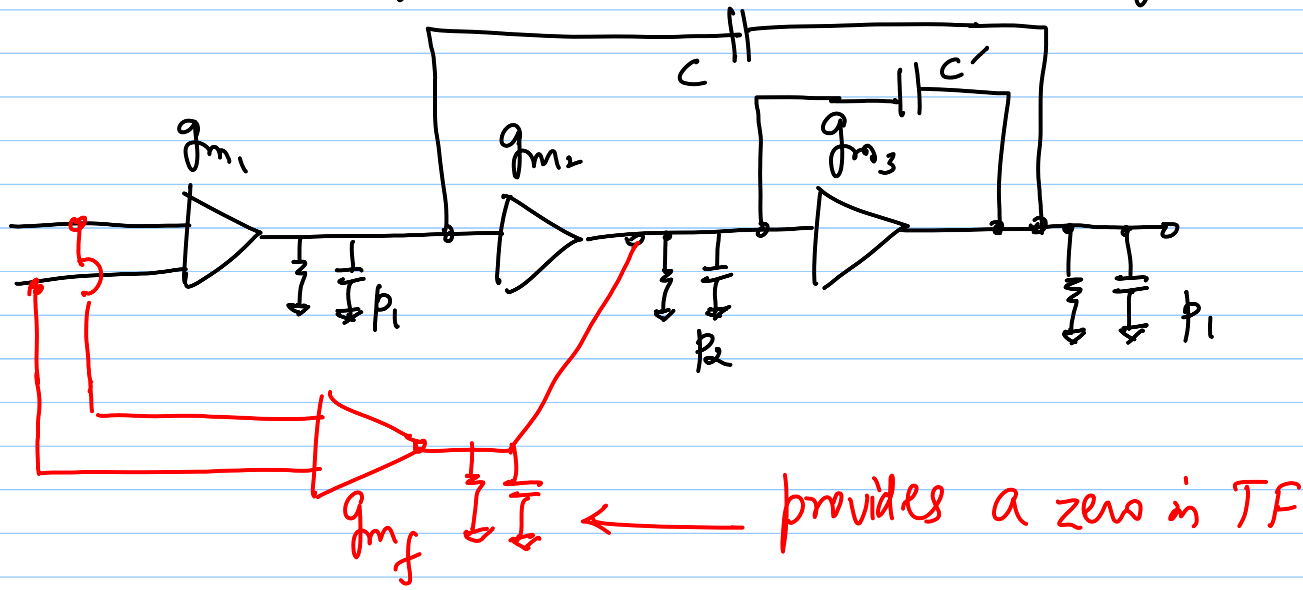
* large gain, but lower speed

$$\omega_u = \frac{g_{m1}}{C} = \frac{1}{4} p_3'$$

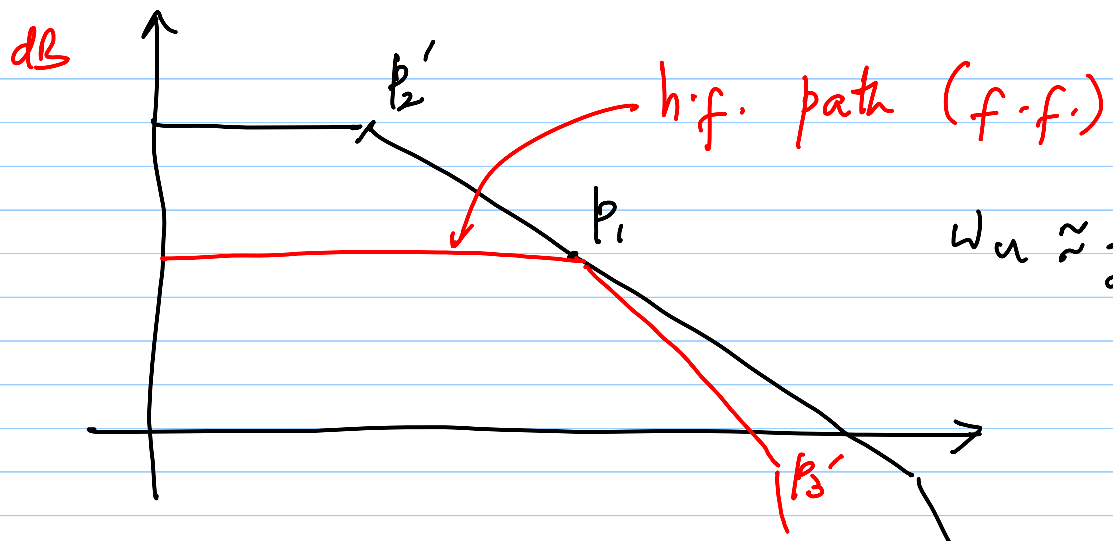
2-stage opamp: $\omega_u = \frac{1}{2} p_3'$

2) <u>Multipath NMC</u> :

* multi-stage with feedforward stages



* c & c' values will be different
* @ low freq. ⇒ main path ; @ high freq. ⇒ f.f. path



$$\omega_u \approx \frac{1}{2} p_3'$$

use ω_z to cancel p_1

$$p_3'' = \frac{p_3'}{2} + \frac{p_3'}{2}\sqrt{1 - \frac{4}{p_3'} \cdot \frac{g_{m_2}}{C'}}$$

$$\frac{g_{m_2}}{C'} = 0 \Rightarrow p_3'' = p_3'$$

$$\frac{g_{m_2}}{C'} \simeq 0.1\, p_3' \text{ is optimal}$$

$\rightarrow$ ~ 10% BW reduction w.r.t. 2-stage

$\rightarrow$ pole-zero trading is implicit over PVT

* g_{mf} adds noise + offset directly @ input

* can move g_{mf} across $g_{m_2} - g_{m_3}$

$\Rightarrow$ g_{mf} must drive V_{out} (slew + settle)

$\Rightarrow$ more power dissipation

* nested + f.f. is also possible

Band gap references

* Reference V/I that are independent of temperature (& therefore process)

Let $V = \alpha_1 V_1 + \alpha_2 V_2$

$$\frac{\partial V}{\partial T} = 0 \Rightarrow \alpha_1 \frac{\partial V_1}{\partial T} + \alpha \frac{\partial V_2}{\partial T} = 0$$

+ve T.C. $\quad\quad$ -ve T.C.

* Bipolar (or diode) BE voltage temp. char:

$$V_{BE} = V_T \ln\left(\frac{I_C}{I_S}\right)$$

$$V_T = kT/q$$

$$I_S \propto \mu k T n_i^2$$

μ = mobility of minority carriers

n_i = intrinsic minority carrier conc. of Si

$$\mu \propto \mu_0 T^m \,, \quad m \approx -3/2$$

$$n_i^2 \propto T^3 \exp\left[-E_g/(kT)\right]$$

E_g = Bandgap energy of Si $\approx$ 1.12 eV

$$\Rightarrow \quad I_S = b T^{4+m} \exp\left[\frac{-E_g}{kT}\right]$$

$$\frac{\partial V_{BE}}{\partial T} = \frac{\partial V_T}{\partial T} \ln \frac{I_C}{I_S} - \frac{V_T}{I_S} \frac{\partial I_S}{\partial T}$$

$$\frac{\partial I_S}{\partial T} = b(4+m)\, T^{3+m} \exp\left[\frac{-E_g}{kT}\right] + b T^{4+m} \exp\left[\frac{-E_g}{kT}\right] \cdot \left(\frac{E_g}{kT^2}\right)$$

$$= \frac{(4+m)}{T} I_S + \frac{E_g}{kT^2} \cdot I_S$$