14-3-12

Lec 28

Design example - contd.

NMOS devices

$\lambda_n L_n = 0.04 \Rightarrow L_n = 1.591\,\mu m$

$\Rightarrow$ choose NMOS lengths $= 2\mu m$ (L_{min})

PMOS devices

$\lambda_p L_p = 0.1 \Rightarrow L_p = 3.978$

use $L_p = 4\mu m$

Checks

1) $g_{m_6} \geq 10\, g_{m_1}$

$g_{m_6} = \sqrt{2 k_p' \left(\frac{W}{L}\right)_6 I_B} = 500\mu S$

$g_{m_1} = 78.5\mu S \Rightarrow g_{m_6} \approx 6.4\, g_{m_1}$

* $\uparrow (W/L)_6$

$\Rightarrow$ parasitic cap $\uparrow$ (x)

$\Rightarrow V_{DSAT_6} \downarrow$ (✓)

$\Rightarrow a_2 \uparrow$ (✓)

* ↑ I_B
  ⇒ V_{DSAT_6} ↑ (x)
  ⇒ a_2 ↑ (✓)
  ⇒ SR ↑ (✓)

  { use combination of ↑ I_6 & ↑ $(W/L)_6$ }

2) Check to see if other poles are ≥ $10\omega_u$

* especially mirror pole from M_3 & M_4

Assume $C_{ox} = 6fF/\mu m^2$

mirror pole $p_3 = \dfrac{-g_{m3}}{2C_{gs_3}} \cdot \dfrac{1}{2\pi}$

$= \dfrac{-\sqrt{2K_p'(W/L)_3 \cdot (I_A/2)}}{(2\pi)\,2\cdot(2/3)\,W_3 L_3 C_{ox}}$

$= 15.55\,MHz \approx 3 f_u$

* ↑ W_3 will ↓ $|p_3|$ X

* ↑ I_A ⇒ $|p_3|$ ↑, but $|p_1|$ will also ↑ (f_u ↑) ...

3) Input CM range

$$V_{ic}(\text{min.}) = V_{GS_1} + V_{DSAT_5}$$

$$= V_{T_1} + 2V_{DSAT} = 2.0V$$

$$V_{ic}(\text{max}) = V_{DD} - V_{SG_3} + V_{T_1}$$

$$= V_{DD} + V_{T_1} - |V_{T_3}| - V_{DSAT_3}$$

$$= 4.5V$$

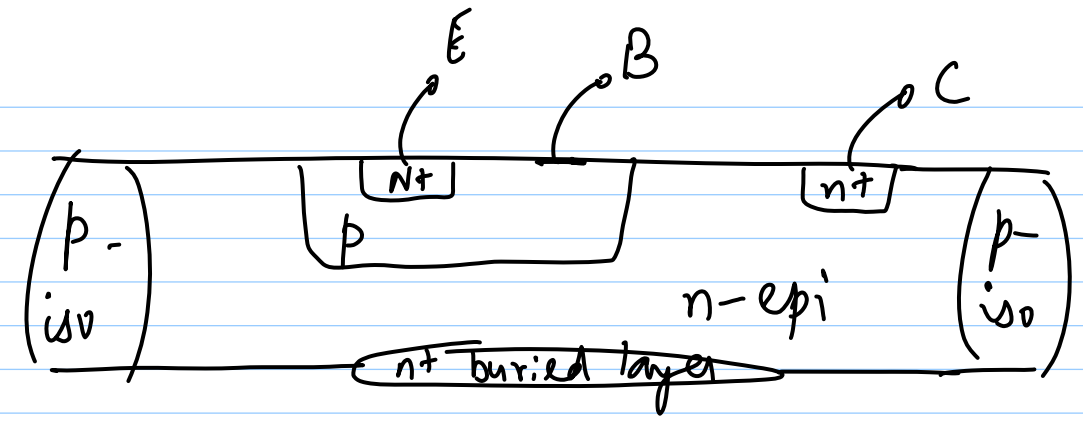
4) Simulation . . .

Bipolar Opamps

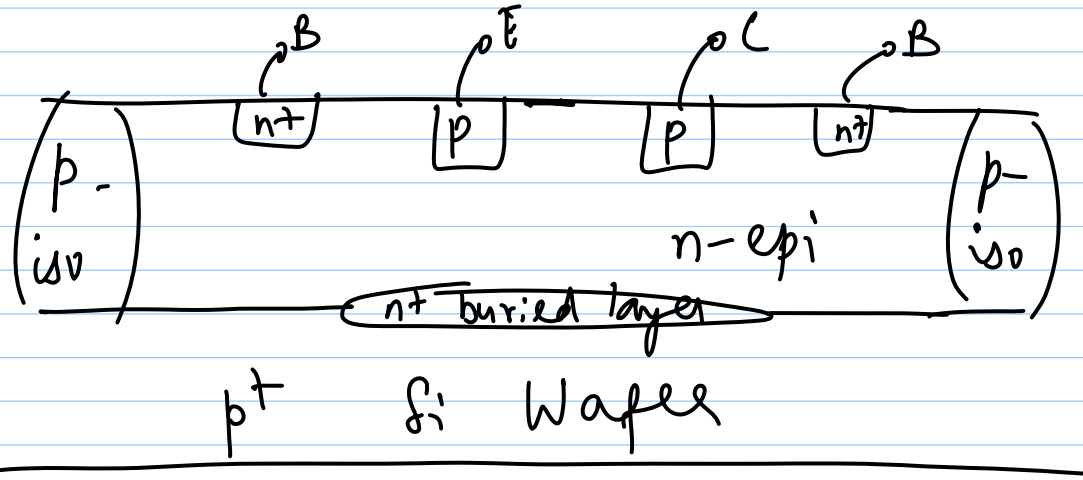
MOS technology → PMOS almost as good as NMOS (complementary)
→ except for $\mu_n - \mu_p$ difference

Bipolar technology → pnp's are inferior to npn

npn – vertical device
pnp – lateral device
) cheaper process



High-speed vertical npn transistor



low-speed low-gain lateral pnp