4/1/12 Lec 2 - Scaling ; MOS Operation

Constant Field Scaling

1) Reduce all lateral & vertical dimensions by α (>1)
   e.g. W, L, t_{ox}, depth & perimeter of S-D junctions

2) Reduce V_{DD} & V_T by α

3) Increase all doping levels by α

① & ② $\Rightarrow$ $\mathcal{E}$-fields inside semiconductor stay constant

Impact on device parameters

1) Current

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_T)^2$$

$$V_{DD} \to V_{DD}/\alpha \Rightarrow V_{GS} \sim V_{GS}/\alpha$$

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} \Rightarrow C_{ox}' = \alpha C_{ox}$$

$$I_D' = \frac{1}{2}\mu_n(\alpha C_{ox}) \cdot \frac{W/\alpha}{L/\alpha} \cdot \left(\frac{V_{GS}}{\alpha} - \frac{V_T}{\alpha}\right)^2$$

$$= \frac{1}{\alpha} I_D$$

2) Capacitance

$$C_{ch} = W L C_{ox}$$

$$C_{ch}' = \frac{1}{\alpha} \cdot C_{ch}$$

Depl. region width

$$W_d = \sqrt{\frac{2 \epsilon_{si}}{q} \left(\frac{1}{N_A} + \frac{1}{N_D} \right) (\phi_B + V_R)}$$

$\phi_B = V_T \ln \left(\frac{N_A N_D}{n_i^2} \right)$, V_R = reverse bias voltage

assume $V_R >> \phi_B$

$$W_d' = \sqrt{\frac{2 \epsilon_{si}}{q} \left(\frac{1}{\alpha N_A} + \frac{1}{\alpha N_D} \right) \cdot \frac{V_R}{\alpha}}$$

$$= \frac{1}{\alpha} \cdot W_d$$

$\Rightarrow$ $C_{depl.}' = \alpha \cdot C_{depl.}$ (||'ar to C_{ox})

Total cap $= C_{depl}' \cdot A' = \frac{1}{\alpha} \cdot C_{depl.}$

in general, all caps $\downarrow$ by α

3) Gate delay (CMOS inv.)

$$T_D = \frac{C}{I} \cdot V_{DD}$$

$$T_D' = \frac{C/\alpha}{I/\alpha} \cdot V_{DD}/\alpha = \frac{1}{\alpha} T_D$$

4) Power Consumption (Digital)

$$P = f\, C\, V_{DD}^2$$

$$P' = f \cdot \frac{C}{\alpha} \cdot \frac{V_{DD}^2}{\alpha^2} = \frac{1}{\alpha^3} \cdot P$$

5) Layout density

$$\text{area}' = \frac{1}{\alpha^2} \cdot (\text{area})$$

6) Transconductance

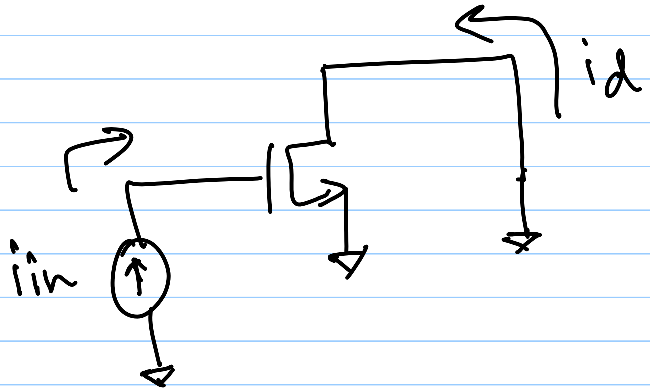
$$g_m = \mu C_{ox} \frac{W}{L} \cdot (V_{GS} - V_T)$$

$$g_m' = \mu(\alpha C_{ox}) \cdot \frac{W/\alpha}{L/\alpha} \left(\frac{V_{GS}}{\alpha} - \frac{V_T}{\alpha}\right)$$

$$= g_m$$

7) $f_T \equiv$ transition frequency

freq. @ which current gain $= 1$



$$\omega_T = 2\pi f_T$$

* neglect C_{db}, r_g

* Effect of C_{gd} only on Z_{in}

$$\left|\frac{i_d}{i_{in}}\right| \simeq \frac{g_m}{\omega(C_{gs}+C_{gd})}$$

ω_T is given by

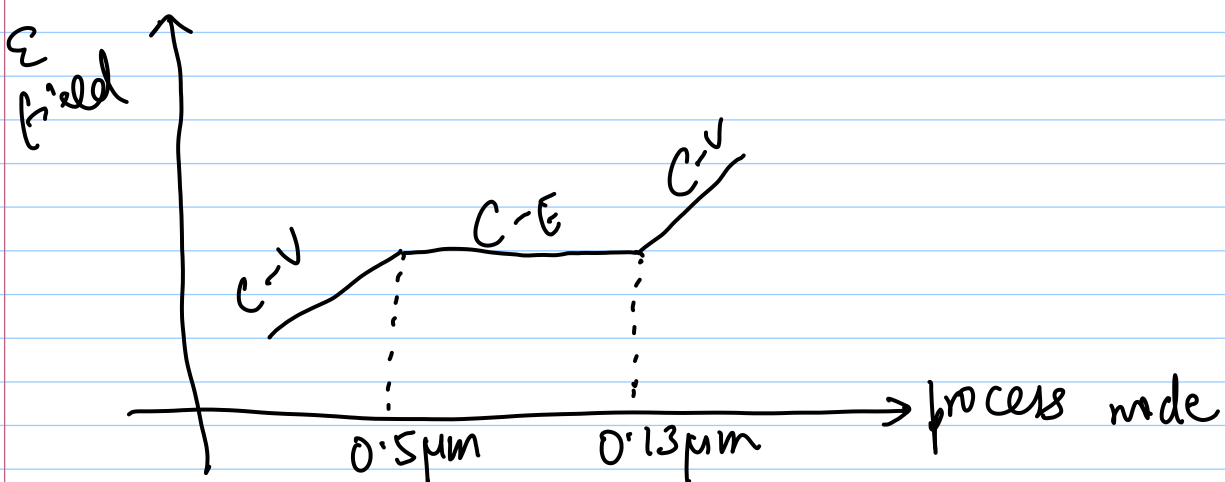
$$\omega_T = \frac{g_m}{C_{gs}+C_{gd}} \simeq \frac{g_m}{C_{gs}}$$

$$\omega_T \simeq \frac{\mu_n C_{ox} \frac{W}{L}(V_{GS}-V_T)}{\frac{2}{3} W \cdot L \cdot C_{ox}}$$

$$= \frac{3}{2}\mu_n \frac{(V_{GS}-V_T)}{L^2} \Rightarrow \underline{\underline{\omega_T' = \alpha\,\omega_T}}$$

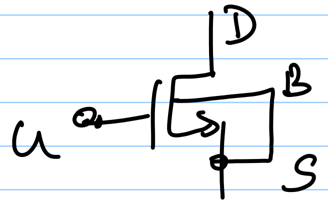
Constant Voltage scaling:

* V = constant
* dimensions are scaled.
  - ⇒ E-field keeps increasing!
  - ⇒ dielectric breakdown can occur

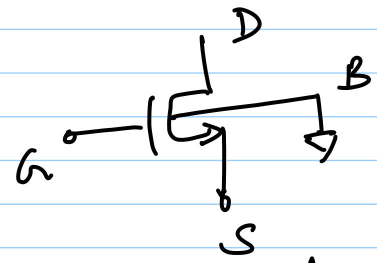


MOS operation – second order Effects

1) Body Effect



vs.



$B = S$ (=gnd, usually)

$$V_{T0} = \phi_{MS} + 2\phi_F + \frac{Q_{depl.}}{C_{ox}}$$

B = gnd, $V_S > V_B$

* S-B depletion region is wider
* larger voltage required @ G to cause inversion

Q_d increases $\Rightarrow$ V_{TH} increases

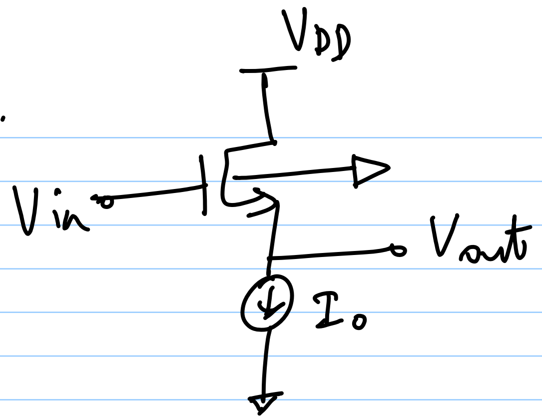
$\Rightarrow$ "Body Effect" or "Backgate Effect"

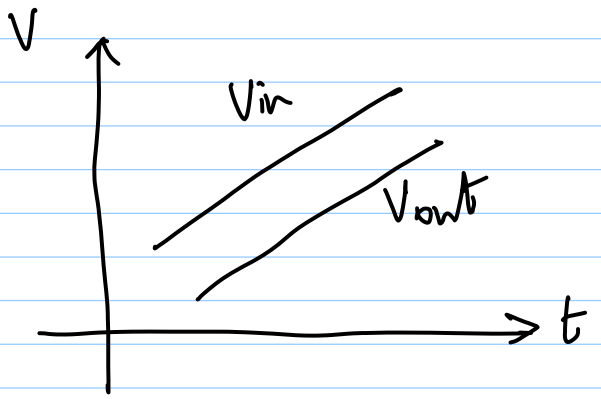
$$V_T = V_{T0} + \gamma\left[\sqrt{|2\phi_F + V_{SB}|} - \sqrt{2\phi_F}\right]$$

$$\phi_F = \frac{kT}{q}\ln\left(\frac{N_{sub}}{n_i}\right)$$ Bulk Fermi potential

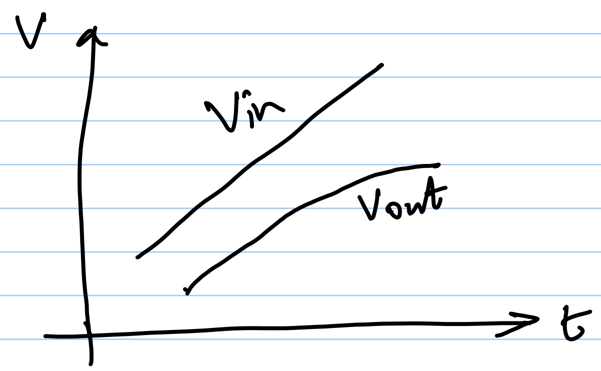
$$\gamma = \frac{\sqrt{2q\epsilon_{si} N_{sub}}}{C_{ox}}$$

e.g.





no body Effect



2) Channel Length Modulation

V_{GD} changes pinch-off point

$\Rightarrow L' = L - \Delta L$

$$\Rightarrow \frac{1}{L'} \simeq \frac{1}{L}\left(1 + \frac{\Delta L}{L}\right)$$

assume $\frac{\delta L}{L} = \lambda V_{DS}$

$$\Rightarrow I_{D_{SAT.}} = \frac{1}{2}\mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T)^2 (1 + \lambda V_{DS})$$

$$g_{ds}\Big|_{sat} = \frac{\partial I_D}{\partial V_{DS}} \simeq \lambda I_D$$

Backgate transconductance :

$$g_{mb} = \frac{\partial I_D}{\partial V_{SB}}\Big|_{V_{DS}, V_{GS}\ \text{const.}}$$

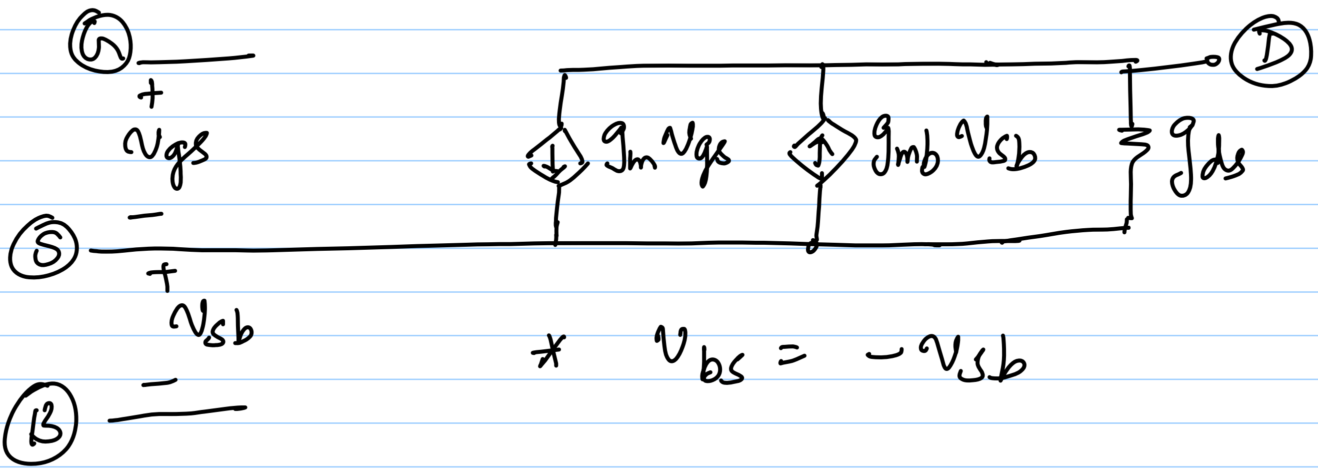
$$= \frac{\partial I_D}{\partial V_T} \cdot \frac{\partial V_T}{\partial V_{SB}} = -\frac{\partial I_D}{\partial V_{GS}} \cdot \frac{\partial V_T}{\partial V_{SB}}$$

$$= -g_m \cdot \frac{\gamma}{2\sqrt{|2\phi_F + V_{SB}|}} = -\eta g_m$$

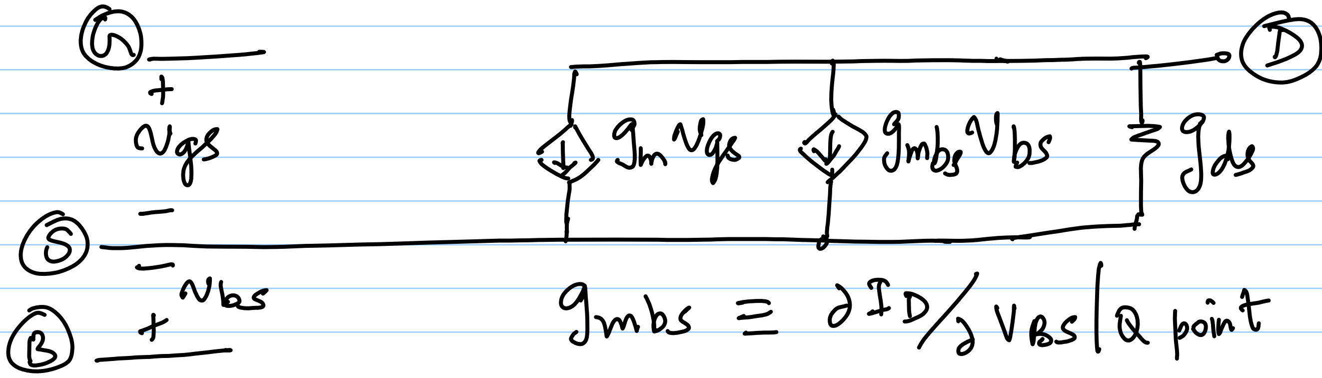
* $-ve$ sign $\Rightarrow$ $i_d \downarrow$ as $v_{sb} \uparrow$

* Typically $0.1 < \eta < 0.2$

* MOSFET small signal model (low freq):



* $v_{bs} = -v_{sb}$



$g_{mbs} \equiv \partial I_D / \partial V_{BS} |_{Q\ point}$

3) Sub-threshold Conduction

$V_{GS} \simeq V_T \Rightarrow$ "weak" inversion layer exists

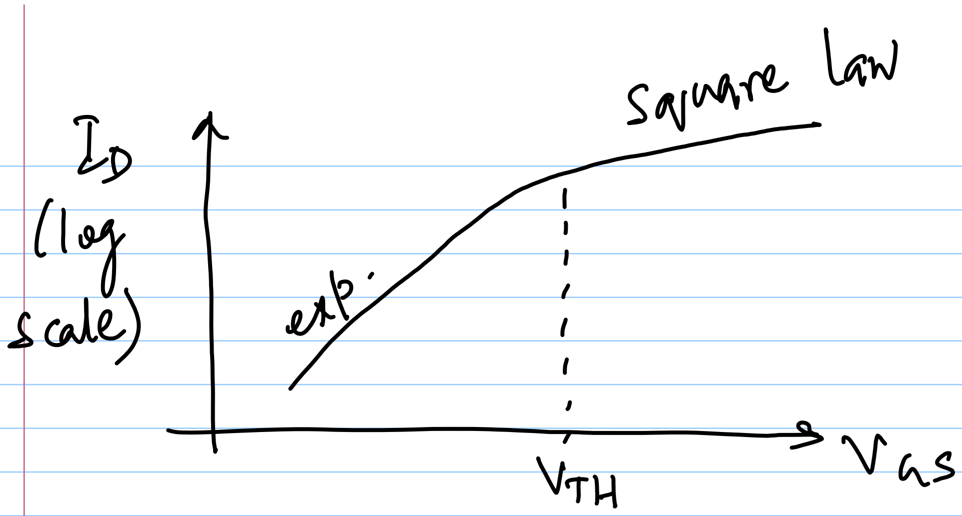
$\Rightarrow I_{DC} \neq 0$

$V_{GS} < V_{TH} \Rightarrow I_D \neq 0$, exponential behaviour

$$I_D = I_0 \exp\left(\frac{V_{GS}}{\zeta V_T}\right)$$ similar to BJT

$\zeta > 1, \quad V_T = \frac{kT}{q}$

* big problem in large dig ckts (power leakage)



$$g_{m_{ST}} = \frac{I_D}{S V_T} < g_{m_{BJT}}$$

* gain is larger in S-T. than sat.

→ speed is limited ! (low f_T)
→ large device (C)
→ low current (I)

Analysis Steps

1) DC op. pt.
   - → Cap O.C.
   - → Use MOS equations $\}$ $I_D = f(V_{GS}, V_{DS})$
   - ⇒ sat, non-sat etc.

2) AC small-signal analysis (in sat. region)
   - → linearised picture
   - → incremental picture ($i, v, r, g \ldots$)