22-2-12

Lec 19

Additional poles & zeroes

* Integrator
* F.b. network

How do you analyse it? (Stability)

* all poles should be in LHP (may be too complicated)

$$\frac{V_o}{V_i}(s) = \frac{1}{f} \cdot \frac{T(s)}{1+T(s)}$$

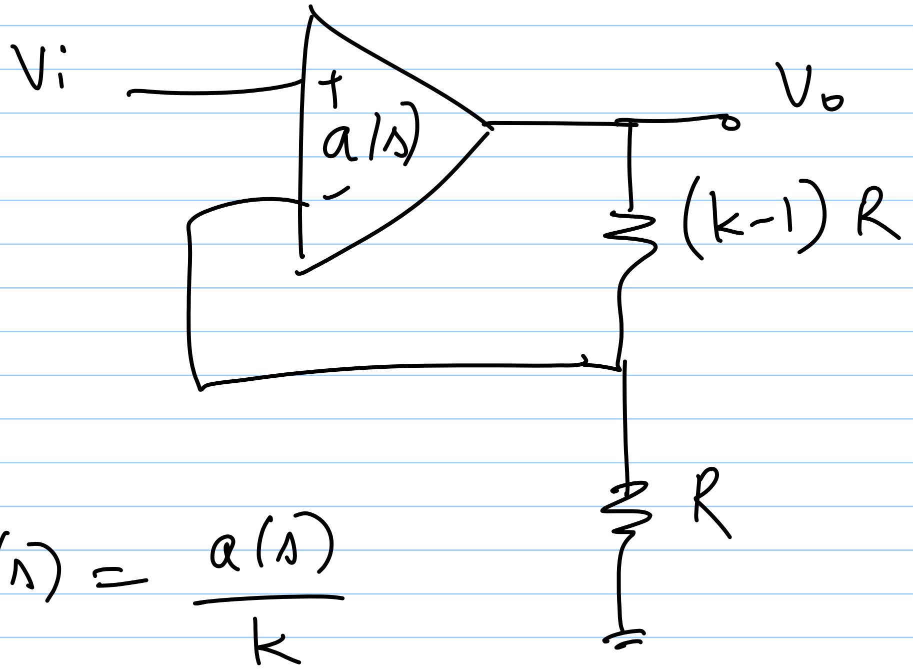
poles of $\frac{V_o}{V_i}(s)$ = zeroes of $1+T(s)$

→ Use Nyquist plot to analyse stability - polar plot of $T(s)$

Tutorial problem on:

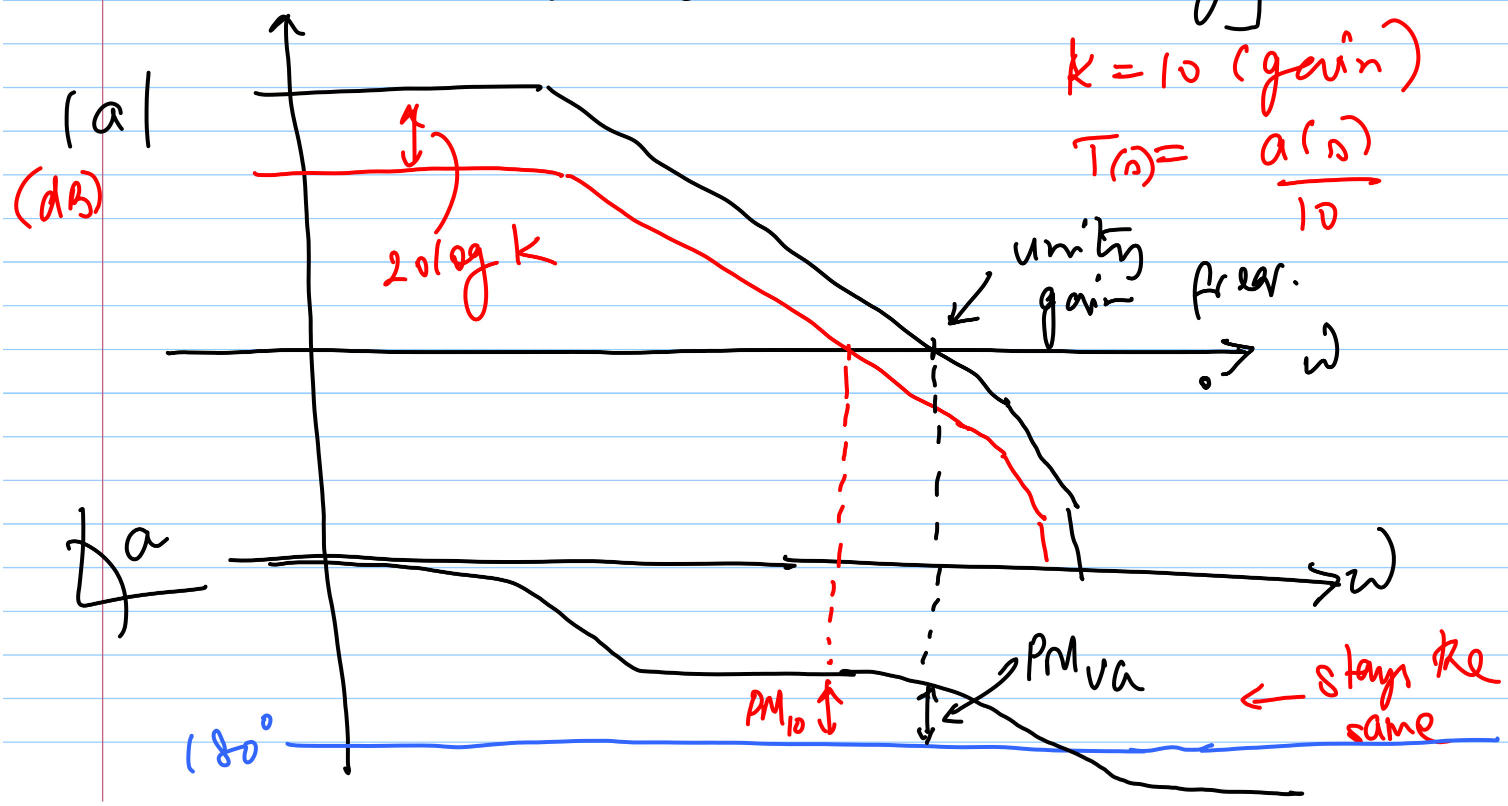
Order	$T(s)$	Unstable?	phase margin
1	$\frac{\omega_{u,loop}}{s}$	No	90°
2	$\frac{\omega_{u,loop}}{s} \cdot \frac{1}{1+\frac{s}{p_2}}$	Stable for: $3<1$ for $p_2 < 4\,\omega_{u,loop}$	76° for $p_2 = 4\,\omega_{u,loop}$
3			
4			

How to design for stability for different gains (k)?



$$T(s) = \frac{a(s)}{k}$$

$a(s)\cdot f$ is what decides stability [not $a(s)$ only]



worst-case:

$\underline{k=1}$ ← highest unity gain freq.

⇒ lowest PM.

assumption: all-pole systems (no zeroes)

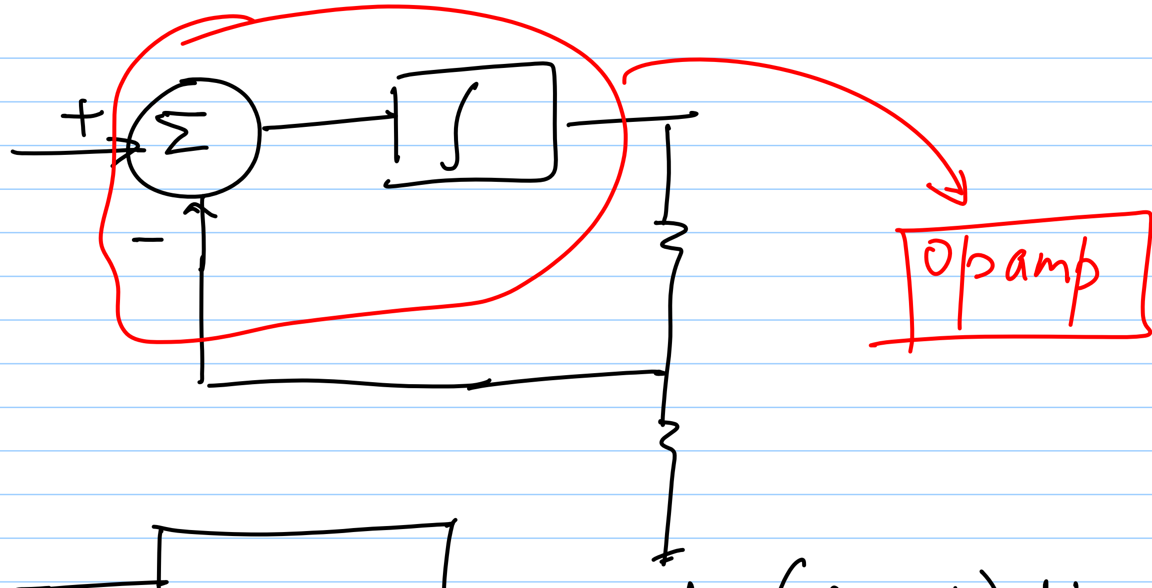
If $a(s)$ satisfies PM condition, other k's will be stable

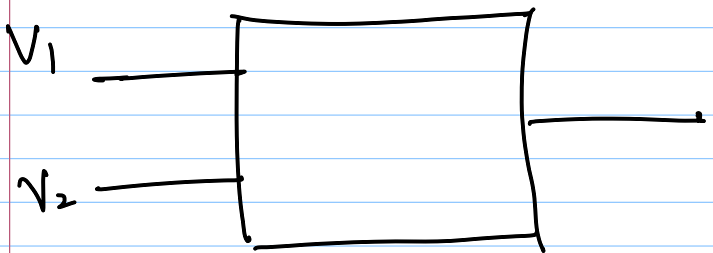
⇒ Unity Gain Compensated Opamp

Many general purpose opamps are UG compensated (e.g. 741)

Issue: Unity gain freq. is lower for higher gain cases

If you know that it is going to be used only in high gain config., can do a custom design for high BW (Typical IC design case)

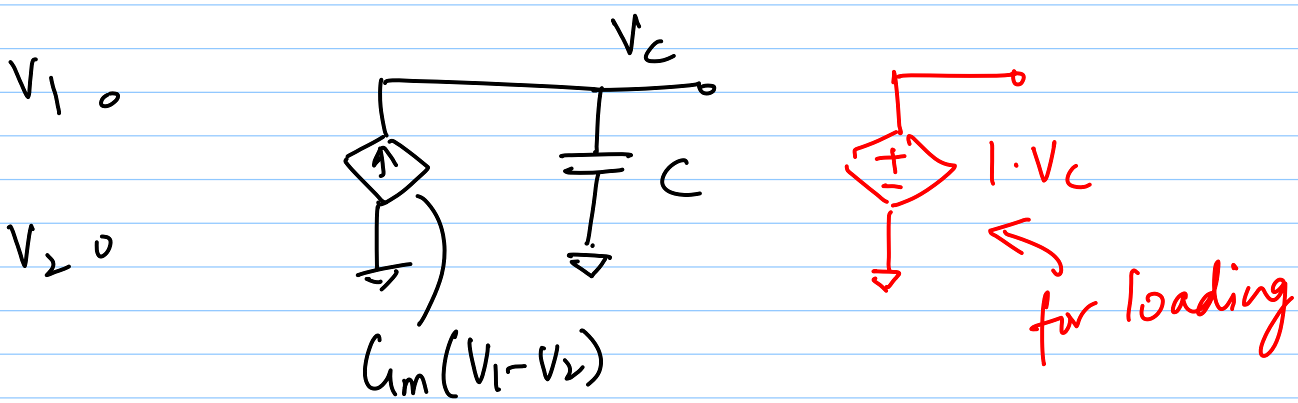




$\omega_u \int (V_1 - V_2)\,dt$

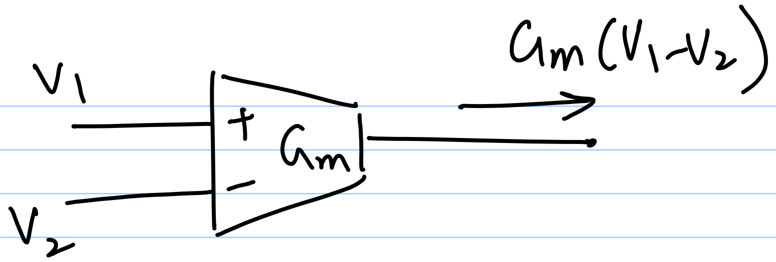
$\int$ = capacitor (inductors are too large)

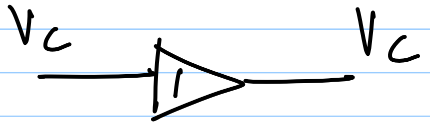
cap integrates I



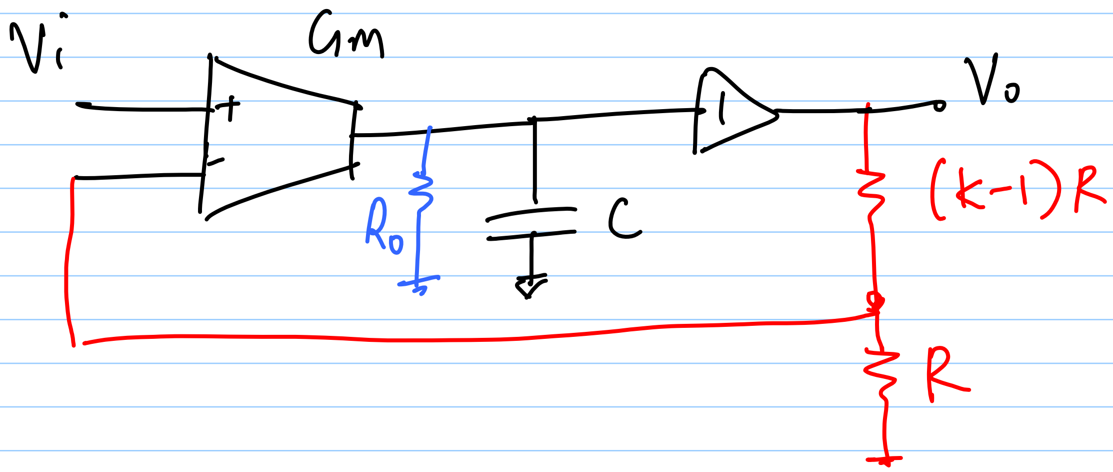
$$V_c = \frac{G_m}{C} \int (V_1 - V_2)\,dt$$

$$\Rightarrow \omega_u = \frac{G_m}{C}$$





buffer



Non-idealities

1) parasitic caps @ nodes : (HW3)
2) Output impedance of G_m- stage

old $$\frac{V_o}{V_i} = \frac{k}{1 + \frac{sC}{G_m}\cdot k}$$

new $$\frac{V_o}{V_i} = \frac{k}{1 + \frac{G_o}{G_m}\cdot k + \frac{sC}{G_m}\cdot k}$$

$$sC \rightarrow sC + G_0$$

$$\left.\frac{V_o}{V_i}\right|_{dc} = \frac{k}{1 + \frac{G_o}{G_m}k} < k$$

finite dc gain

$V_i =$ unit step

$$\text{error} = \frac{1}{1 + \frac{G_o}{G_m}k}$$

Opamp

$$\frac{G_m}{sC} \rightarrow \frac{G_m}{sC + G_o}$$

$$\omega_u \Rightarrow \frac{G_m}{\sqrt{\omega^2 C^2 + G_o^2}} = 1$$

or

$$\frac{1}{\frac{\omega^2 C^2}{G_m^2} + \frac{G_o^2}{G_m^2}} = 1 \quad \left(\frac{G_o^2}{G_m^2} \rightarrow 0\right)$$

What should G_o be?

$$\frac{V_o}{V_i} \rightarrow k \Rightarrow \frac{G_o}{G_m} \cdot k \ll 1$$

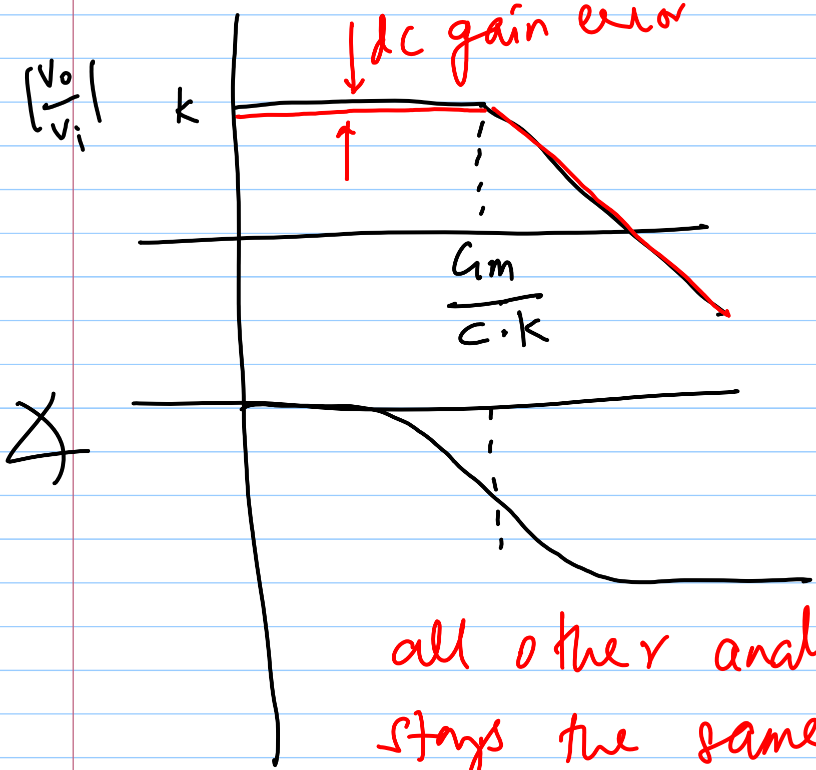
$$\Rightarrow G_o \ll \frac{G_m}{k}$$

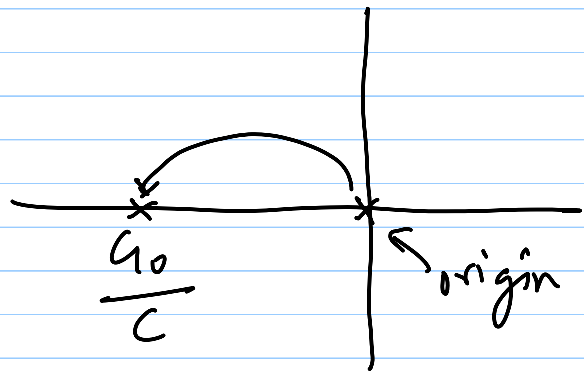
$$\text{or} \quad \frac{G_m}{G_o} \gg k$$

e.g. error in $k < 1\%$; $k = 10$

$$\Rightarrow 1 + \frac{G_o}{G_m} \cdot k \simeq 1.01$$

$$\Rightarrow \frac{G_m}{G_o} = 1000$$



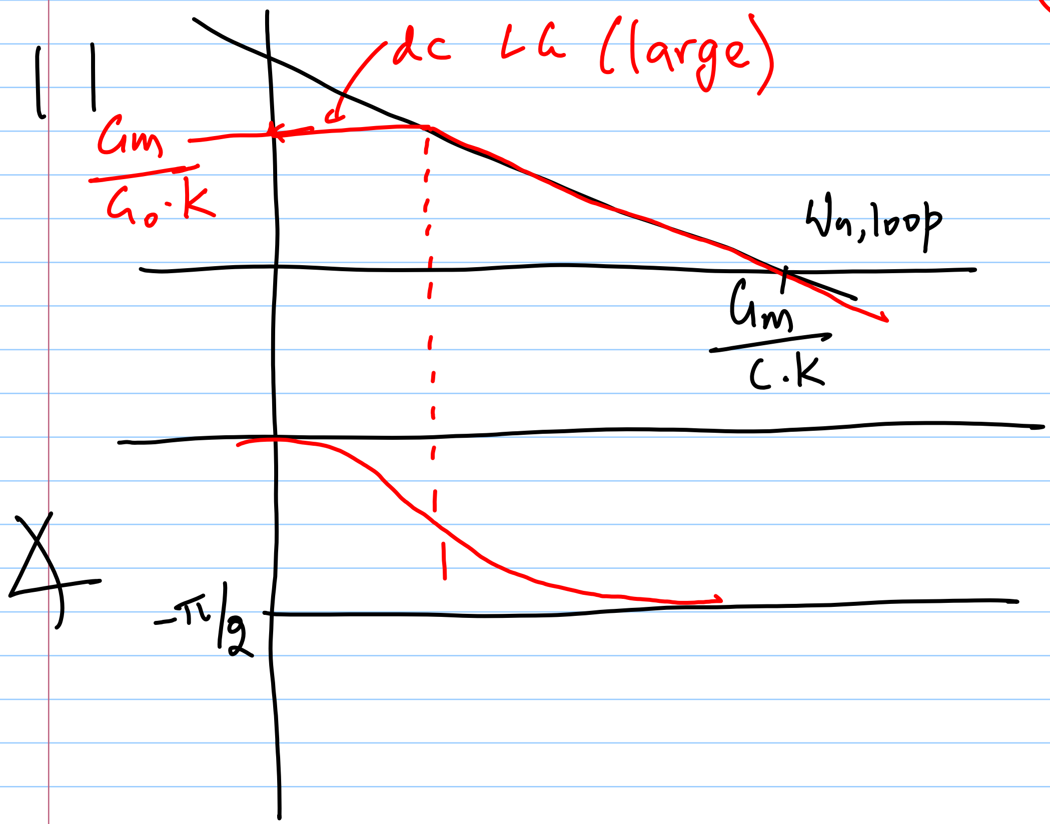


all other analysis stays the same

$\frac{V_o}{V_i}$ went from

$$\frac{k}{1 + \frac{sC}{G_m} \cdot k} \rightarrow \frac{k}{1 + \frac{sC}{G_m} \cdot k + \frac{G_o}{G_m} \cdot k}$$

Loop gain: $\frac{G_m}{sC \cdot K} \rightarrow \frac{G_m}{(sC + G_o) \cdot K}$



Finite dc gain : because $R_o \neq \infty$

* $\frac{\omega_u}{s} \rightarrow \frac{1}{\frac{s}{\omega_u} + \frac{1}{A_o}}$ ← A_o: dc gain

* steady state gain error
  relative error $\approx \frac{1}{DC\ LG}$

* How to increase $\frac{G_m}{G_o}$?
  $G_o \Rightarrow$ typically from r_{ds}

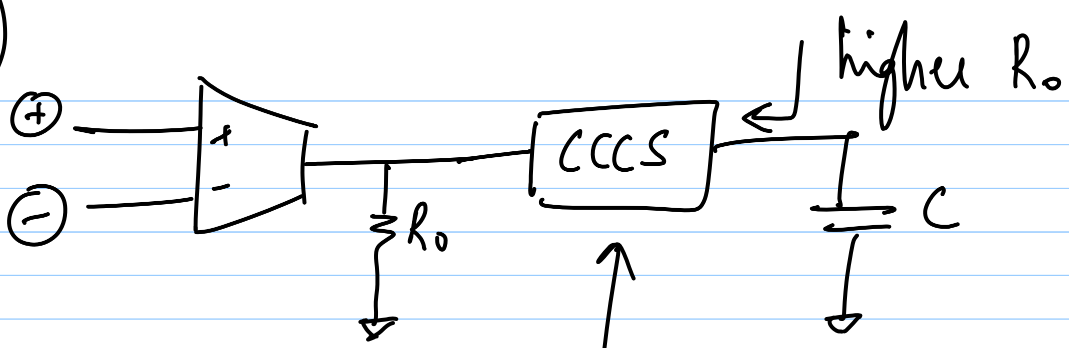
→ dependence on I (reduce)
but $G_m \downarrow \Rightarrow G_m/C \downarrow$

→ dependence on L (increase)
but area ↑ too; also C will increase due to device cap

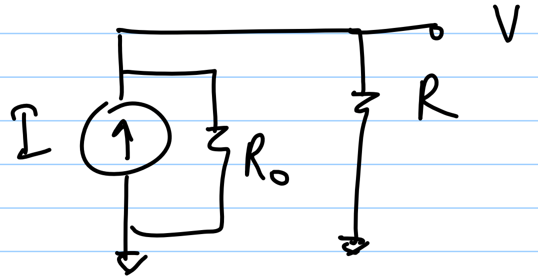
Cannot ↑ by large factors (e.g. 100 times)

Basic problem: all of $G_m \cdot \Delta V_{in}$ current does not flow thro' cap

1)



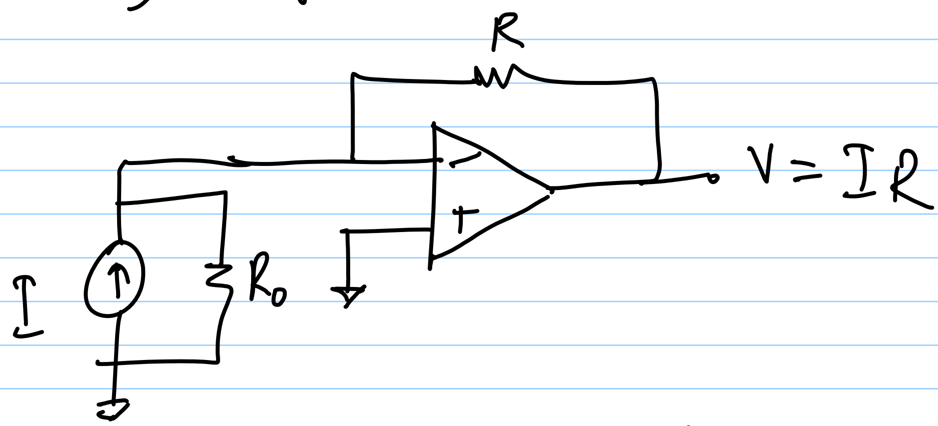
2) I-V converter.

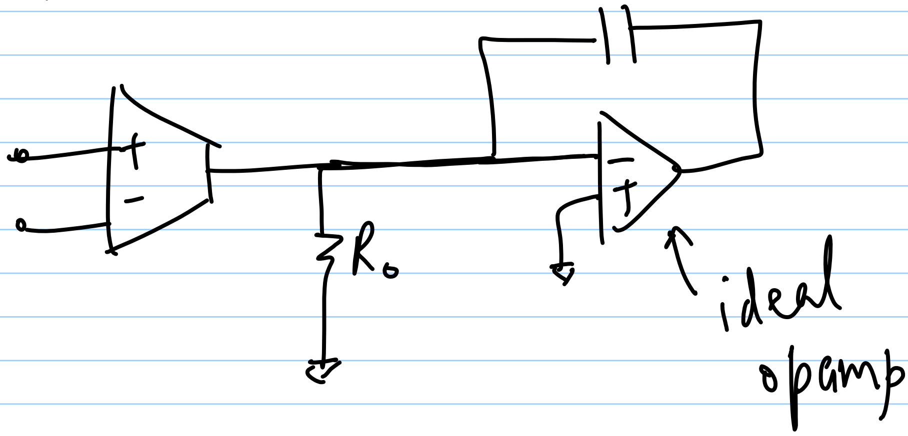


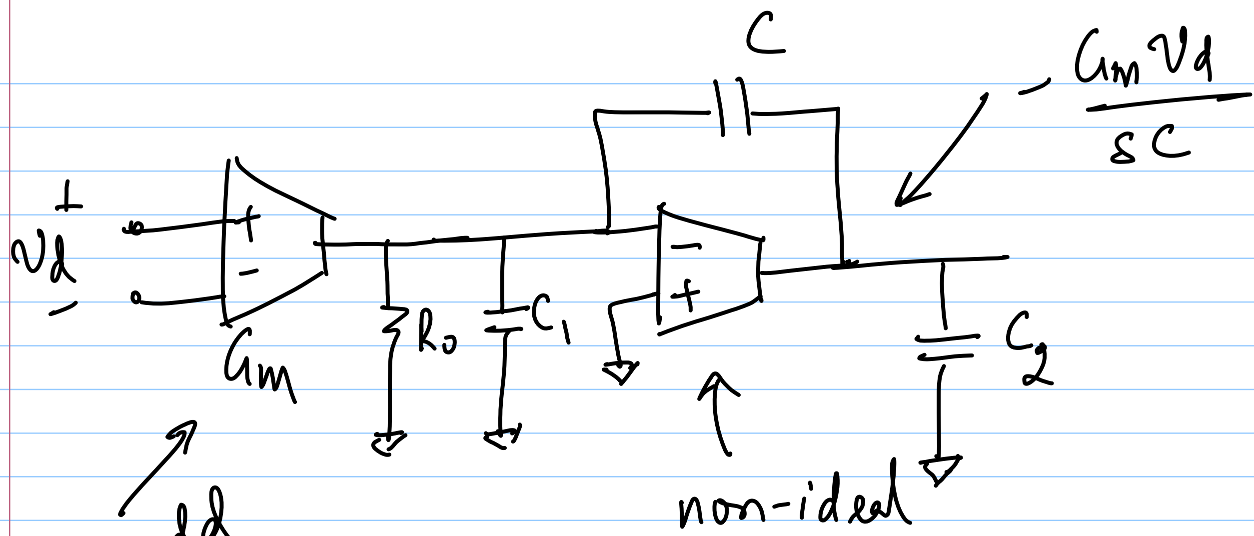
If $R_o < \infty$,

$V < IR$

⇒ use a CCVS



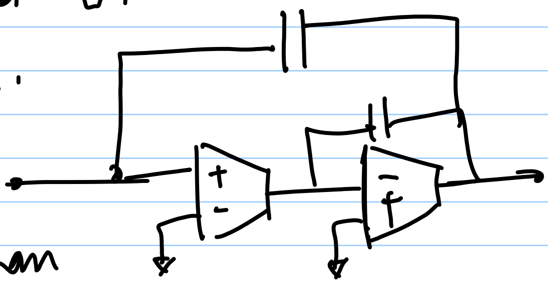




can add CCCS to improve Gm stage

can be replaced with more complex arch.

e.g.



typically not more than 3-stages

problem : each Gm has R_o

each node has C

⇒ extra delay

<u>Opamp</u>

→ Differencing of voltage $(V_1 - V_2)$

→ integration of $V_1 - V_2$

⇒ transconductor + capacitor

→ R_o ⇒ finite DC gain
- → ↑ L
- → ↑ R_o (CCCS
- → transimp. amp. (I-V)