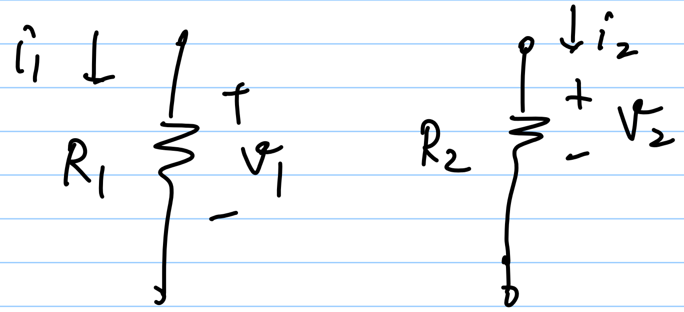
31/1/12

Lec 12

Half-ckt analysis with mismatch:



$$i_d = i_1 - i_2$$

$$i_c = \frac{i_1 + i_2}{2}$$

$$\Delta R = R_1 - R_2$$

$$R = (R_1 + R_2)/2$$

$$v_d = v_1 - v_2 = i_1 R_1 - i_2 R_2$$

$$v_c = \frac{v_1 + v_2}{2} = \frac{i_1 R_1 + i_2 R_2}{2}$$

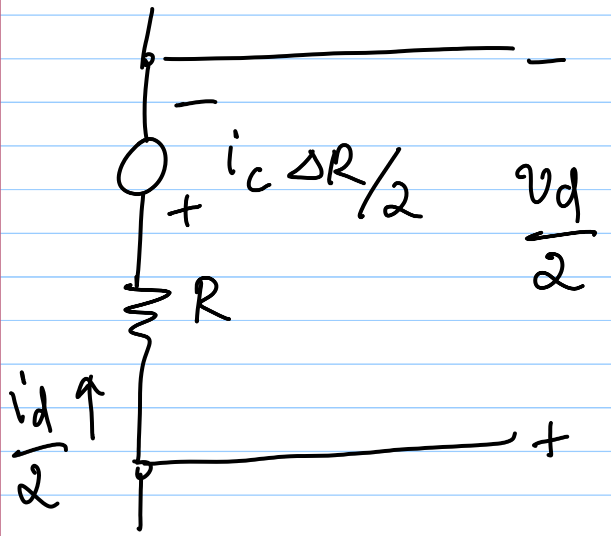
$$v_d = \left(i_c + \frac{i_d}{2}\right)\left(R + \frac{\Delta R}{2}\right) - \left(i_c - \frac{i_d}{2}\right)\left(R - \frac{\Delta R}{2}\right)$$

$$\simeq i_d R + i_c (\Delta R)$$

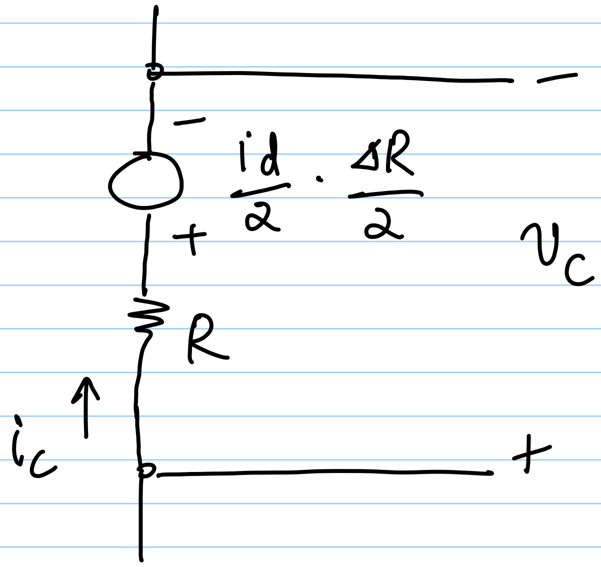
$$v_c = \frac{(i_c + i_d/2)(R + \Delta R/2) + \left(i_c - \frac{i_d}{2}\right)(R - \Delta R/2)}{2}$$

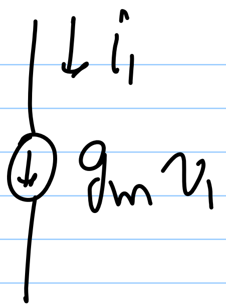
$$\simeq i_c R + \frac{i_d (\Delta R)}{4}$$

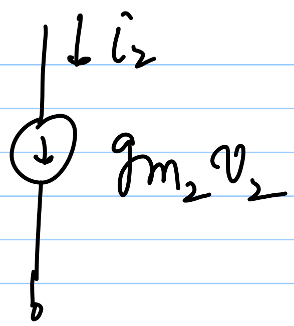
Diff half cct:

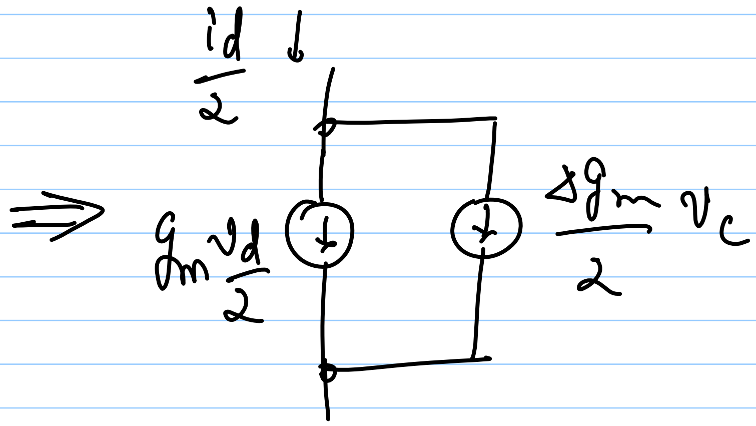


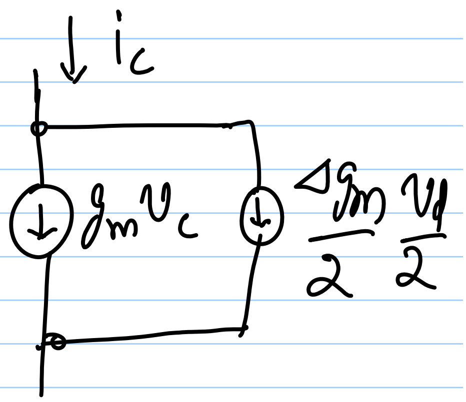
Cm half cct:









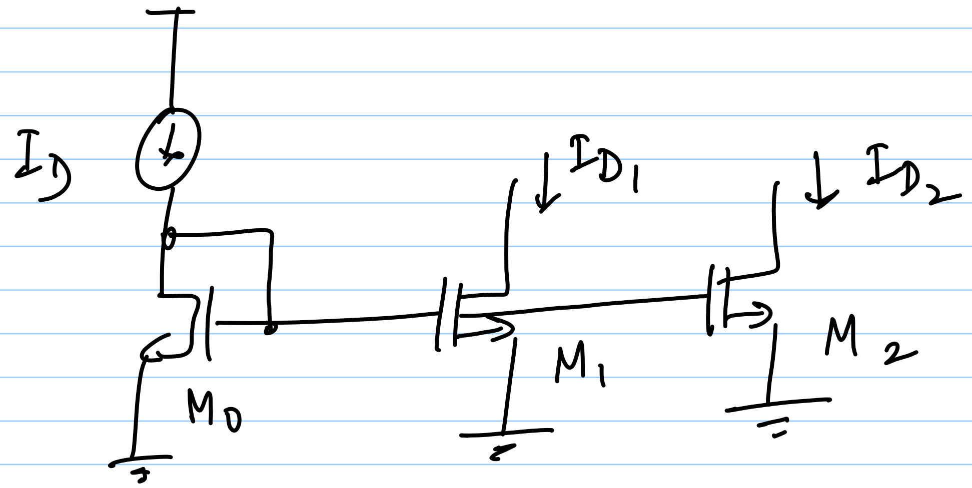


Diff. H.C.

$$\Rightarrow \quad \{A_{dm},\ A_{cm}\},\ \{A_{cm-dm},\ A_{dm-cm}\}$$

$A_{dm} = \dfrac{v_{od}}{v_{id}}$, $A_{cm} = \dfrac{v_{oc}}{v_{ic}}$, $A_{cm-dm} = v_{od}/v_{ic}$, $A_{dm-cm} = v_{oc}/v_{id}$

Current source mismatch:



$$I_D = \frac{\beta}{2}\left(\frac{W}{L}\right)(V_{GS}-V_T)^2$$

$$\Delta I_D = \frac{\partial I_D}{\partial (W/L)}\,\Delta\left(\frac{W}{L}\right) + \frac{\partial I_D}{\partial (V_{GS}-V_T)}\cdot \Delta(V_{GS}-V_T)$$

$$= \frac{1}{2}\beta\left(\frac{W}{L}\right)(V_{GS}-V_T)^2 \cdot \Delta\left(\frac{W}{L}\right) - \beta\left(W/L\right)(V_{GS}-V_T)\cdot \Delta V_T$$

$$\frac{\Delta I_D}{I_D} = \frac{\Delta (W/L)}{(W/L)} - 2\,\frac{\Delta V_T}{(V_{GS}-V_T)}$$

⇒ to minimise current mismatch, maximise $(V_{GS}-V_T)$

* Dependence of V_{OS} on $(V_{GS}-V_T)$ is similar to that of noise

→ $\overline{v^2_{n,in}}$ (diff pair) $\propto \frac{1}{g_m} = \frac{V_{GS}-V_T}{2I_D}$

→ $\overline{v^2_{n,out}}$ (CM) $\propto g_m = \frac{2I_D}{V_{GS}-V_T}$

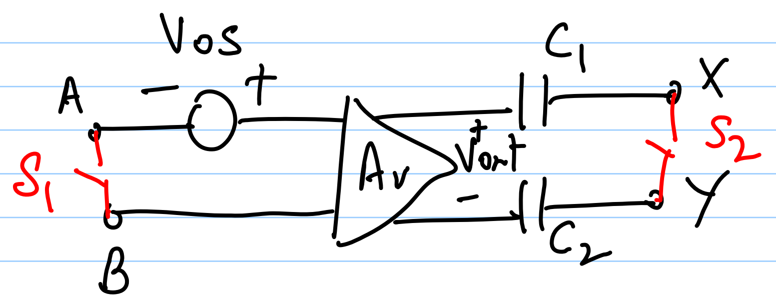
Offset Cancellation

Why?

to reduce V_{OS} ⇒ reduce $(V_{GS}-V_T)$

⇒ larger devices ⇒ larger C_{in}

⇒ lower speed and/or higher P_{diss}



* If S_1 & S_2 are ON,

$$V_{out} = A_V \cdot V_{OS}$$

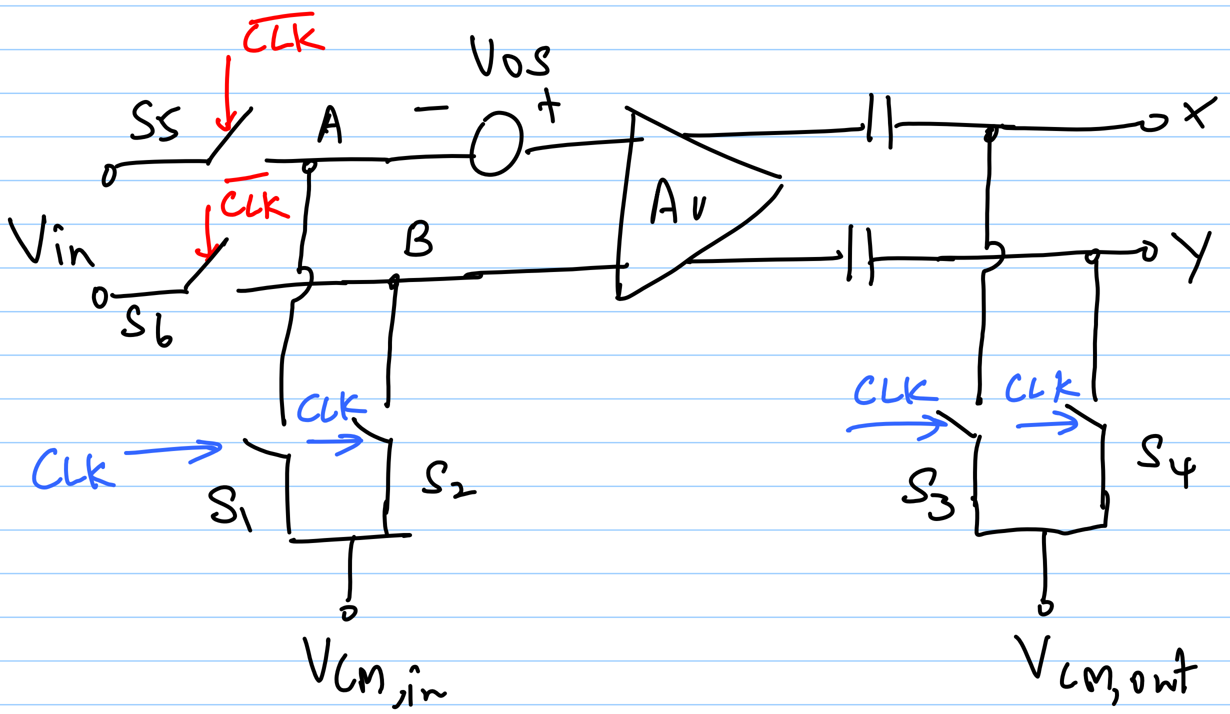
⇒ since $V_{XY} = 0$, $A_V \cdot V_{OS}$ is stored across C_1, C_2

i.e. $V_{AB} = 0 \implies V_{XY} = 0$

Now turn off S_1, S_2

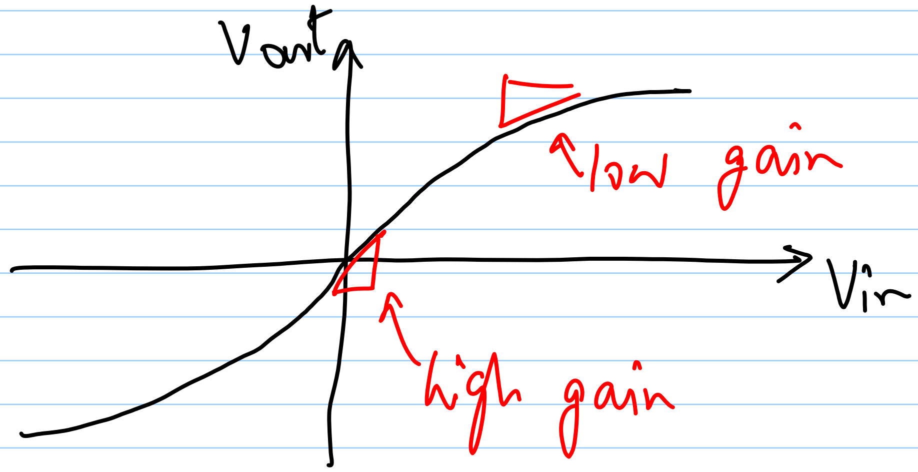
⇒ overall (amp + C_1-C_2) combo exhibits zero offsets

In practice:

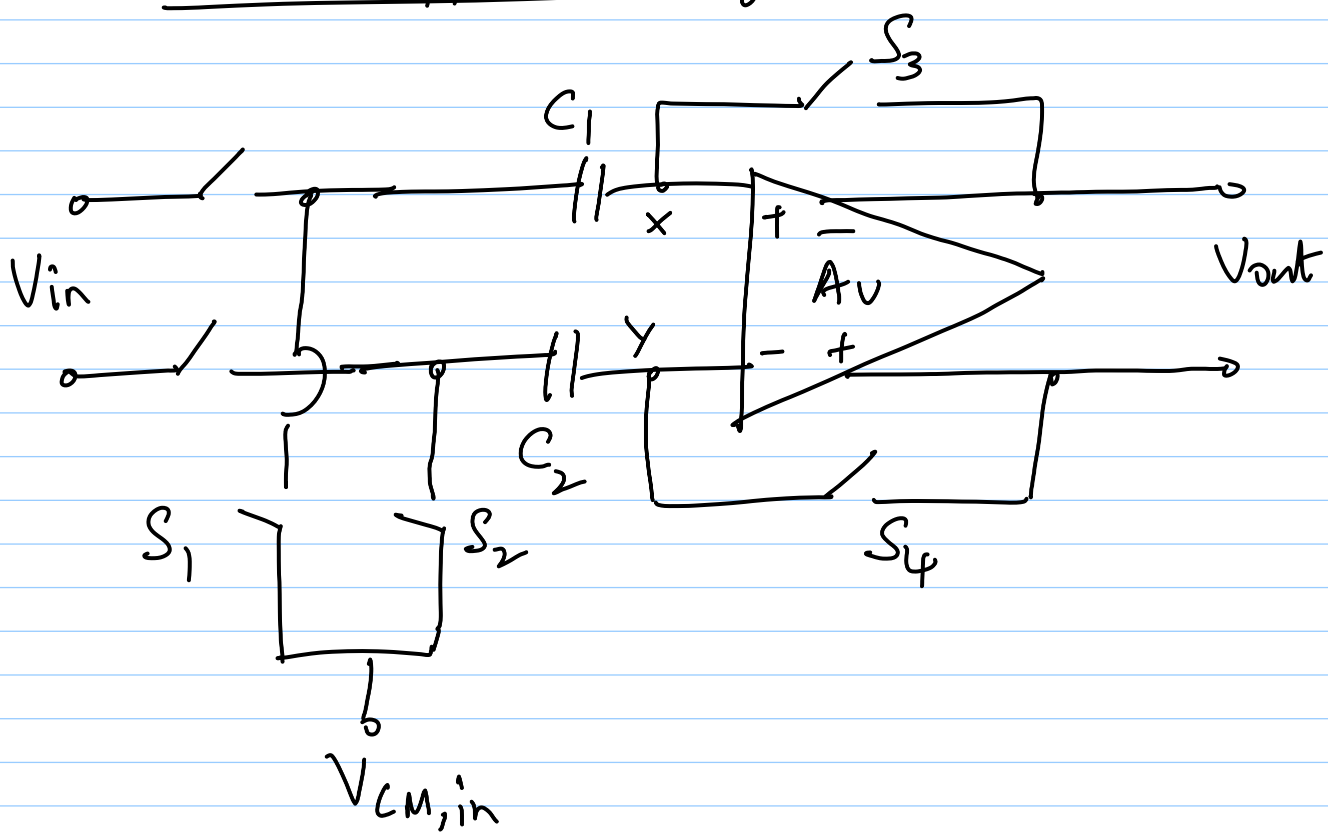


⇒ Output offset storage

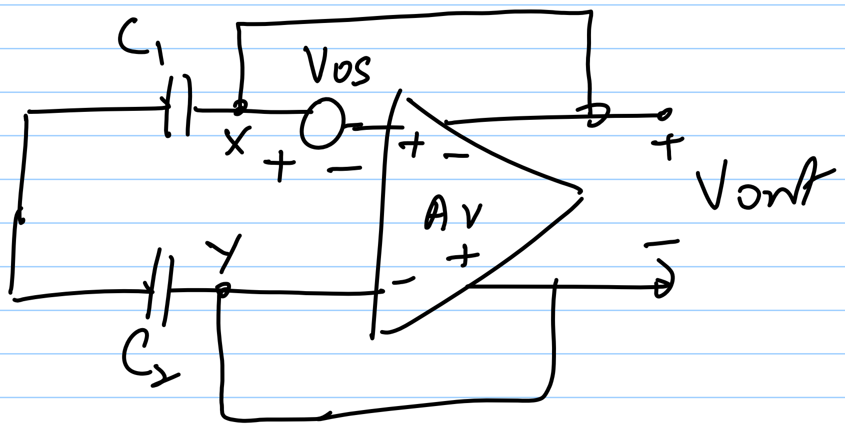
* fine for low-gain stages
What happens if A_v is too large?
$V_{out} = A_v \cdot V_{os}$ can "saturate" the amplifier



Input-offset storage



When $S_1 - S_4$ are closed:



Unity gain config.

$$V_{XY} = V_{out}$$

$$\Rightarrow V_{out} = (-A_V)(V_{out} - V_{OS})$$

$$\Rightarrow V_{out} = \frac{A_V}{1+A_V} \cdot V_{OS} \approx V_{OS}$$

$$\Rightarrow V_{XY} \approx V_{OS}$$

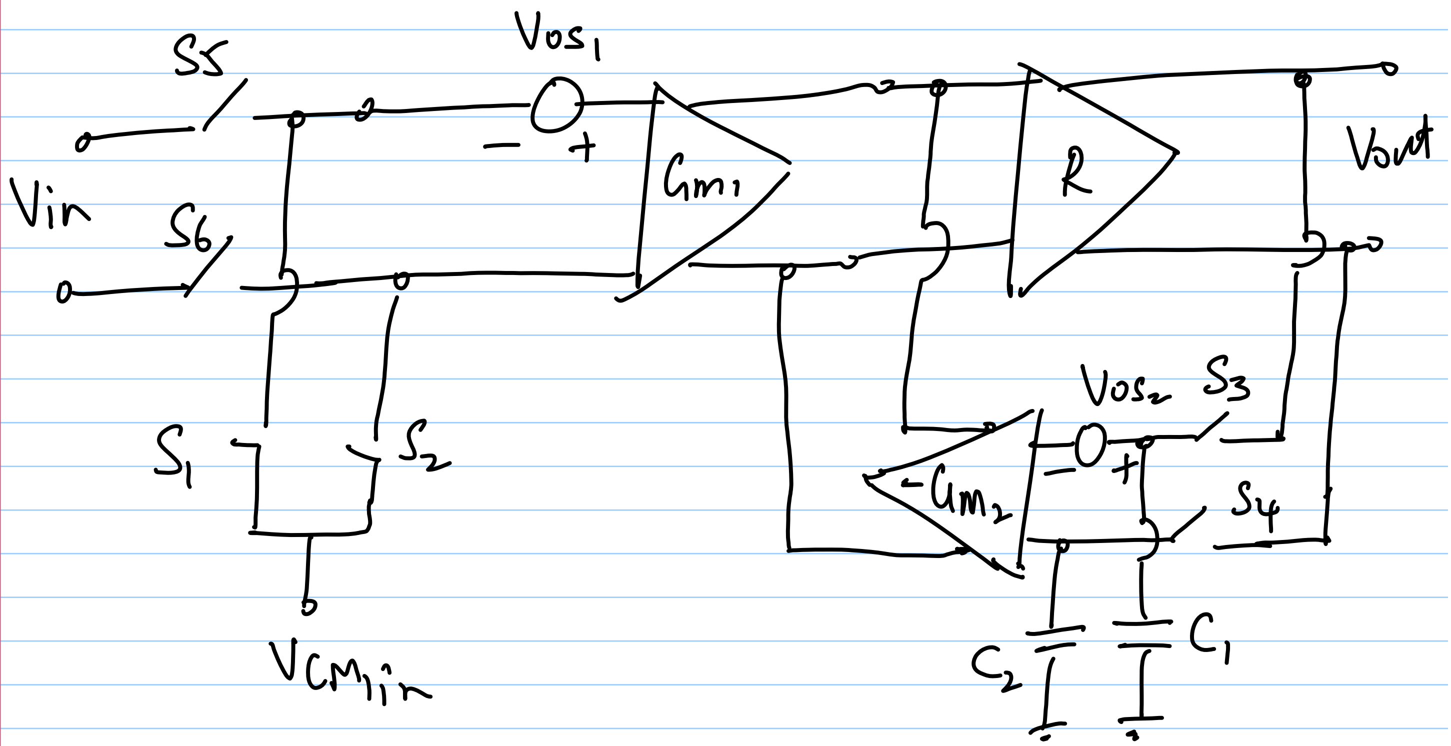
Offset voltage is stored on $C_1 - C_2$

* Both techniques introduce caps in signal path

→ cap parasitics degrade phase margin

→ limits settling speed

Aux. Amp



* Gm stages : currents are easier to add

Phase 1 : $S_1 - S_4$ are ON, $S_5 - S_6$ OFF

$$\left\{ G_{m_1} \cdot V_{os_1} - G_{m_2}\left(V_{out} - V_{os_2}\right) \right\} \cdot R = V_{out}$$

$$\Rightarrow V_{out} = \frac{G_{m_1} R V_{os_1} + G_{m_2} R V_{os_2}}{1 + G_{m_2} R}$$

this is stored on C_1, C_2

Phase 2 : $S_1 - S_4$ are off, $S_5 - S_6$ ON

$$V_{os,tot.} = V_{out} / (G_{m_1} R)$$

$$= \frac{V_{OS_1}}{1+G_{m_2}R} + \frac{G_{m_2}}{G_{m_1}} \frac{V_{OS_2}}{1+G_{m_2}R}$$

$$\simeq \frac{V_{OS_1}}{G_{m_2}R} + \frac{V_{OS_2}}{G_{m_1}R}$$

* Assume amplifier offset cancellation happens @ every sampling operation

→ Can show that noise @ low freq. also gets cancelled
(freq. depends on sampling freq. f_s)