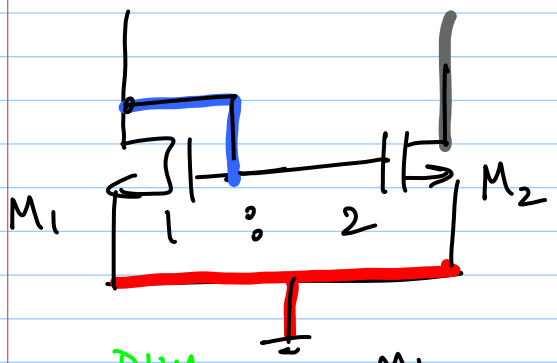
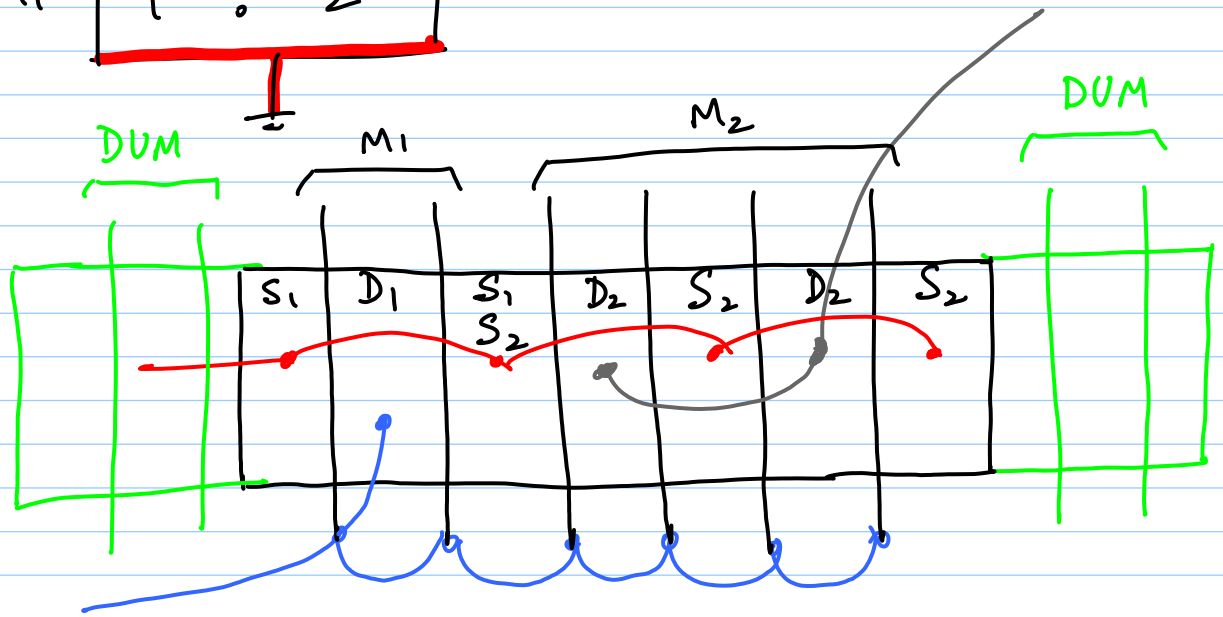
27-1-12

Lec 11



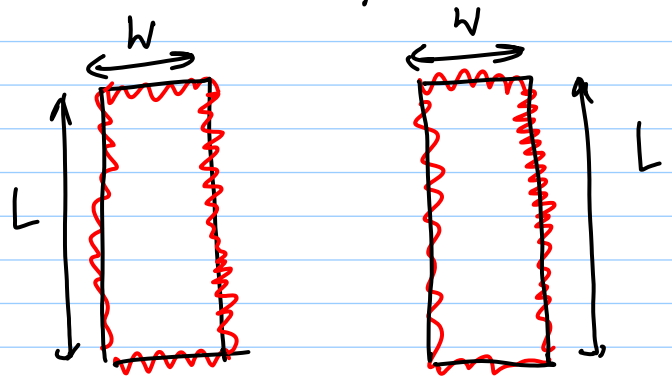
* typically connect dummies to gnd



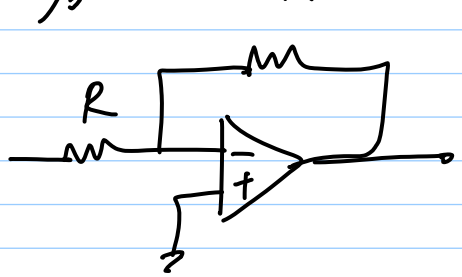
Random Mismatch

R_{sh} : $100\,\Omega/\square$ $\pm$ 30%

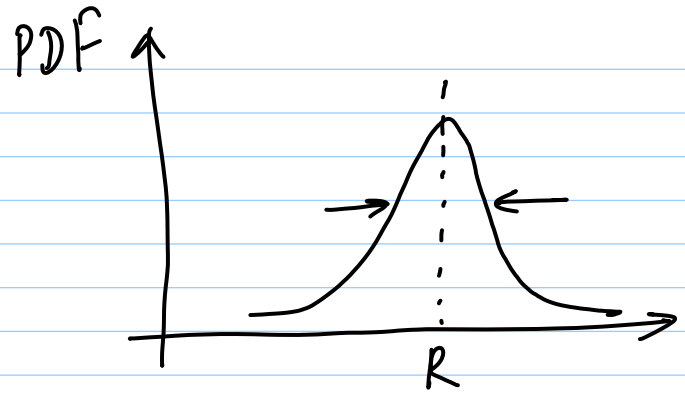
C : $1\,fF/\mu m^2$ $\pm$ 20%



R $\quad$ R + ΔR



identical structures have different values



$(\mu \pm \sigma) \Rightarrow 68\%$

$(\mu \pm 2\sigma) \Rightarrow 95\%$

$(\mu \pm 3\sigma) \Rightarrow 99.7\%$

$= R_{SH} \cdot \left(\frac{L}{W}\right)$

$$I_D = \frac{1}{2} \mu C_{ox} \left(\frac{W}{L}\right) \left(V_{hs} - V_T\right)^2$$

components : μ, C_{ox}, W, L, V_T

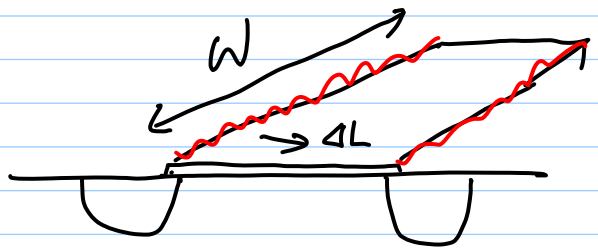
Observations:

* as $W, L \uparrow \Rightarrow \frac{\Delta W}{W} \& \frac{\Delta L}{L} \downarrow$

$\Rightarrow$ larger device exhibit smaller mismathes

* as $(W \cdot L) \uparrow$, $\frac{\Delta W}{W} \& \frac{\Delta L}{L} \downarrow$

e.g. as $W \uparrow$, $\frac{\Delta L}{L} \downarrow$ due to "averaging" effect



* Averaging: view devices as parallel combination of many smaller ones

$$W = W_0 \cdot n \quad \{n \text{ parallel devices}\}$$

$$L_{eq.} = \frac{1}{n}\sum_{i=1}^{n} L_i$$

Overall variation:

$$\Delta L_{eq.} = \frac{1}{n}\sqrt{\sum_{i=1}^{n} \Delta L_i^2}$$

$$\approx \frac{1}{n}\sqrt{n\,\Delta L_0^2} = \frac{\Delta L_0}{\sqrt{n}}$$

$\Rightarrow$ i.e. if L_0 is statistical variation of length for width W_0, increasing n decreases overall $\Delta L_{eq.}$

* Similarly, μ, C_{ox} & V_T also show decreased mismatches when $(WL)\uparrow$.

$$\sigma_{V_T} = \frac{A_{V_T}}{\sqrt{WL}}$$

e.g. $A_{V_T} = 5\,mV.\mu m$

$$\sigma_\beta = \frac{A_\beta}{\sqrt{WL}}$$

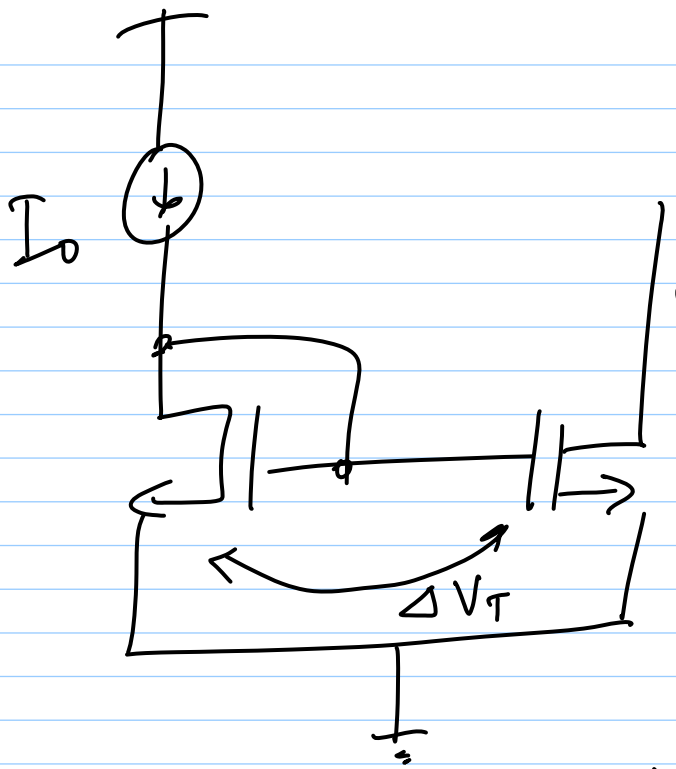
$\beta = \mu C_{ox}$

Similarly, $\sigma\left(\frac{\Delta R}{R}\right) = \frac{A_R}{\sqrt{WL}}$

$\sigma\left(\frac{\Delta C}{C}\right) = \frac{A_C}{\sqrt{WL}}$

} averaging effects in R, C also

$A_R, A_C \rightarrow \%\cdot\mu m$ (units)



$$\Delta I = -g_m \Delta V_T$$

$$\sigma^2(\Delta I) = g_m^2 \sigma_{V_T}^2$$

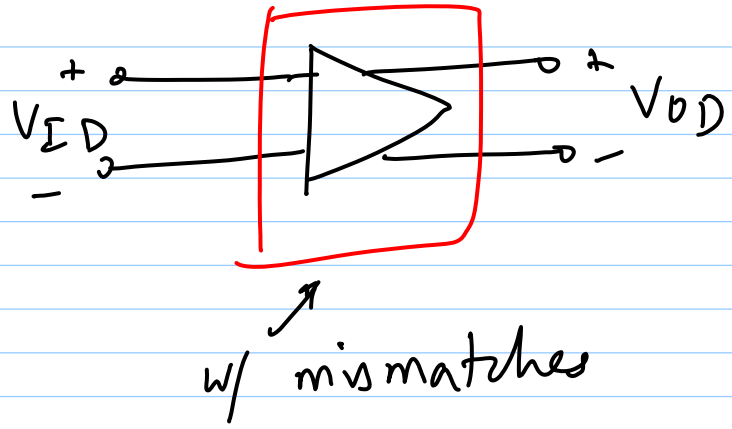
$$\sigma^2\left(\frac{\Delta I}{I_0}\right) = \frac{g_m^2}{I_0^2}\sigma_{V_T}^2$$

$$= \frac{4\sigma_{V_T}^2}{(V_{GS}-V_T)^2}$$

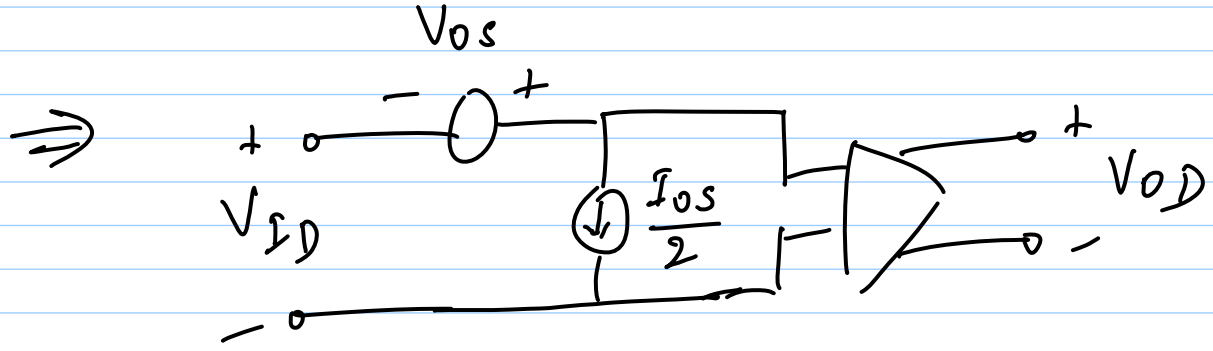
$$= \frac{2\mu C_{ox}}{I_0}\left(\frac{A_{V_T}}{L^2}\right)$$

Effects of mismatch:

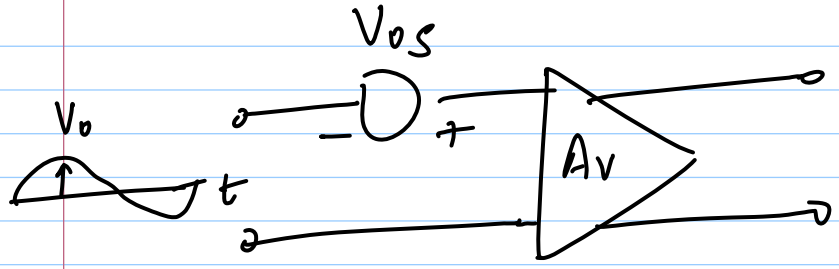
* DC offsets
* Even-order distortion {ideally gets cancelled, but due to mismatches ...}

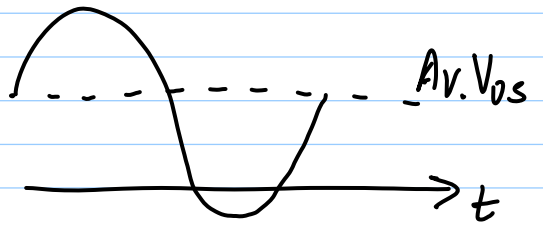


w/ mismatches



(valid for any source Res.)

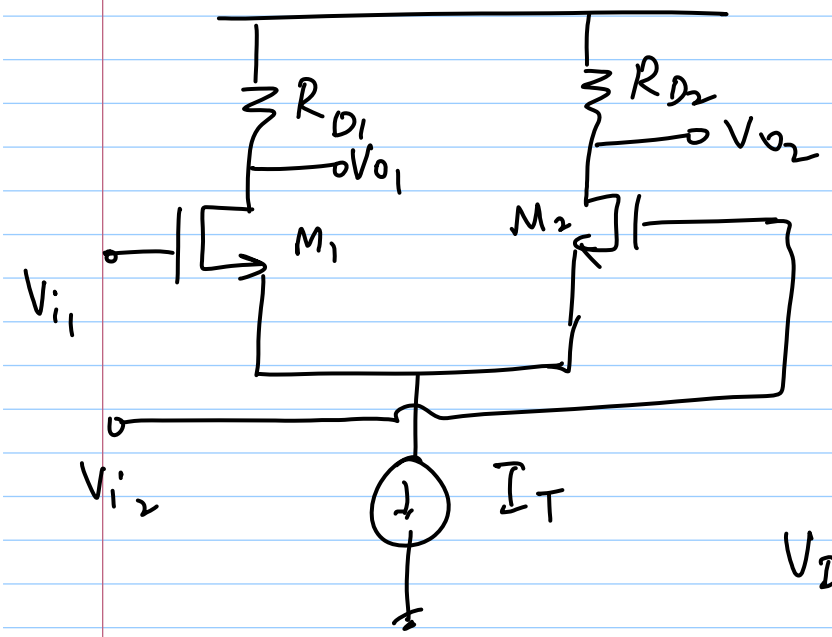




non-linearities

* Can saturate cascade of gain stages
* DC offsets can be time-varying
  e.g. with temperature
* DC offsets can limit minimum V_{in} that can be detected

MOS Diff-pair



DC quantities

$V_{ID} = V_{I_1} - V_{I_2}$

$M_1 - M_2$, $R_{D_1} - R_{D_2}$ } not identical

$V_{ID} = V_{GS_1} + V_{GS_2}$

$I_{OS} = 0$ (All gate currents = 0)

$$V_{ID} = V_{T_1} + \sqrt{\frac{2I_{D_1}}{\beta\left(\frac{W}{L}\right)_1}} - V_{T_2} - \sqrt{\frac{2I_{D_2}}{\beta(W/L)_2}}$$

Input offset voltage

$V_{OS} \equiv$ voltage to be applied to input to drive V_{OD} to 0

$V_{OD} = 0 \Rightarrow I_{D_1} R_{D_1} = I_{D_2} R_{D_2}$ (constraint)

* for small mismatches, an approx analysis can be done

$$\Delta I_D = I_{D_1} - I_{D_2}$$

$$I_D = \frac{I_{D_1} + I_{D_2}}{2}$$

$$\Delta(W/L) = (W/L)_1 - \left(\frac{W}{L}\right)_2$$

$$(W/L) = \frac{(W/L)_1 + (W/L)_2}{2}$$

$$\Delta V_T = V_{T_1} - V_{T_2}$$

$$V_T = (V_{T_1} + V_{T_2})/2$$

$$\Delta R_D = R_{D_1} - R_{D_2}$$

$$R_D = (R_{D_1} + R_{D_2})/2$$

You can write

$$I_{D_1} = I_D + \frac{\Delta I_D}{2} \; ; \; I_{D_2} = I_D - \frac{\Delta I_D}{2}$$

$$(W/L)_1 = (W/L) + \frac{\Delta(W/L)}{2}$$

$$(W/L)_2 = (W/L) - \frac{\Delta(W/L)}{2}$$

$\therefore$

$$V_{OS} = \Delta V_T + \sqrt{\frac{2(I_D + \Delta I_D/2)}{\beta\left[(W/L) + \frac{1}{2}\Delta(W/L)\right]}}$$

$$- \sqrt{\frac{2(I_D - \Delta I_D/2)}{\beta\left[\left(\frac{W}{L}\right) - \frac{1}{2}\Delta\left(\frac{W}{L}\right)\right]}}$$

$$= \Delta V_T + (V_{GS} - V_T)\left[\sqrt{\frac{1 + \Delta I_D/(2I_D)}{1 + \frac{\Delta(W/L)}{2(W/L)}}}\right.$$

$$- \left[\frac{1 - \Delta I_D/(2I_D)}{1 - \frac{\Delta(W/L)}{2(W/L)}} \right]$$

Simplifies to:

$$V_{OS} = \Delta V_T + \frac{(V_{GS} - V_T)}{2} \left(\frac{\Delta I_D}{I_D} - \frac{\Delta(W/L)}{W/L} \right)$$

also $I_{D_1} R_{D_1} = I_{D_2} R_{D_2}$

$$\Rightarrow I_D R_D = (I_D + \Delta I_D)(R_D + \Delta R_D)$$

$$\Rightarrow I_D R_D \simeq I_D R_D + R_D \Delta I_D + I_D \Delta R_D$$

$$\Rightarrow \frac{\Delta I_D}{I_D} = - \frac{\Delta R_D}{R_D}$$

$$\therefore V_{OS} = \Delta V_T + \frac{(V_{GS} - V_T)}{2} \left(- \frac{\Delta R_D}{R_D} - \frac{\Delta W/L}{W/L} \right)$$

* minimize $(V_{GS} - V_T)$ to reduce V_{OS}
* ΔV_T is directly referred to output
* MOS V_{OS} > BJT V_{OS}

Since mismatches are independent:

$$\sigma_{V_{OS}}^2 = \left(\frac{V_{GS}-V_T}{2}\right)^2 \cdot \left[\sigma_{\frac{\Delta R_D}{R_D}}^2 + \sigma_{\left(\frac{\Delta W/L}{W/L}\right)}^2\right]$$

$$+ \sigma_{V_T}^2$$