EE6240 Project 4: VCO Design – due Thursday 17/11/2011

In this project, you are asked to design a fully-differential LC-VCO that meets or exceeds the specifications given below. Use the IBM 0.13µm CMOS process parameters supplied to you through the class website. You will have to use real inductors, designed and modeled using ASITIC.

(a) Design the VCO for the following specs:

- f_0 = 2.4GHz
- V_{DD} = 1.2V
- Tuning range >= 15%
- Minimum output amplitude (differential) = 0.7V
- Phase noise = -100dBc/Hz @ 100kHz offset and -135dBc/Hz @ 3MHz offset
- Maximum number of inductors/transformers = 2; Maximum diameter of each is 200µm
- Tune using MOS transistor based varactors
- Minimise power consumption (P_{diss})

Make sure to include a Kvco plot as well as VCO transient simulation output.

(b) Now, combine the VCO from (a) above with the LNA-Mixer combo you designed in Project 3 – part (b). Determine the overall Gain, NF and IIP_3 and compare your results to hand calculations.

Notes:

1. Grading will be relative to all three VCO performance metrics: Phase noise, Tuning Range, and P_{diss}. However, note that a design meeting the first two specs and having least P_{diss} is the most preferable situation.
2. Explicitly bias any gates using a current mirror to generate the V_{bias} {i.e. do not use a voltage source of V_{bias} at the gate}. Also, connect <u>all NMOS bulks</u> to ground. Connecting them locally to the sources is not allowed.
3. Include and discuss your VCO design procedure and architecture choice in your report.