EE6240 Project 3: Mixer Design – due Monday 24/10/2011

In this project, you are asked to design a fully-differential double-balanced direct-conversion mixer that meets or exceeds the specifications given below. Use the IBM 0.13µm CMOS process parameters supplied to you through the class website. Assume a single-ended RF signal at the input, and use an ideal balun to perform single-ended to differential conversion to drive the mixer transconductance stage. There are three steps in the project:

(a) In this portion of the project, model any inductors in your mixer (except for the ideal balun) with equivalent parallel RLC circuits having Q = 10 at the desired frequency of operation f_0 and self-resonant frequency $f_{sr} = 5f_0$. Design the mixer for the following specs:

- f_{RF} = 2.401GHz; f_{LO} = 2.4GHz (to test the baseband output at 1MHz)
- V_{DD} = 1.2V
- G_C > 15dB
- SSB NF ≤ 13dB; model γ = 2, δ = 4 for the devices in the transconductor portion
- IIP_2 ≥ 40dBm; use two tones at 2.405Ghz and 2.406GHz and apply a mismatch of 1% between all devices (active or passive) in the differential paths
- IIP_3 ≥ 5dBm; use two tones at 2.405Ghz and 2.406GHz
- Minimise power consumption (P_{diss})

(b) Now, combine the mixer from (a) above with the LNA you designed in Project 1 – part (a). Determine the overall Gain, NF and IIP_3 and compare your results to hand calculations.

(c) If you have any inductors in your design, model them using ASITIC, and show final mixer performance with these inductor models. If you do not have any inductors, you are done after (b).

Notes:

1. Grading will be relative to all four mixer performance metrics: Gain (G_C), SSB NF, IIP_3 and P_{diss}. However, note that a design meeting the first three specs and having least P_{diss} is the most preferable situation.
2. Explicitly bias the transconductor gates using a current mirror to generate the V_{bias} {i.e. do not use a voltage source of V_{bias} at the gate}. Also, connect all NMOS bulks to ground. Connecting them locally to the sources is not allowed.
3. It is expected that the IM2 and IM3 components be well-behaved with normal linear behaviour at low power levels and gain compression at high powers. Some gain-expansion is ok, but too much is not good. Make sure your IM2 and IM3 curves do not have any unexpected non-linearities at lower power levels.
4. Include and discuss the expected characteristics of the LO waveform in your report.