EE6240 Project 2: LNA Design – due Wednesday 28/09/2011

In this project, you are asked to design a single-ended Low-Noise Amplifier for the specifications given below. You are allowed to choose any reasonable LNA circuit topology (including those not discussed in class). Use the IBM 0.13µm CMOS process parameters supplied to you through the class website. There are two steps in the project:

(a) In this portion of the project, model all inductors in your LNA with equivalent parallel RLC circuits having Q = 10 at the desired frequency of operation f_0 and self-resonant frequency $f_{sr} = 5f_0$; no ideal inductors are allowed! Design for the following specs:

- $R_{in} = 50\Omega$; tuned output {assume mixer input cap of 100fF in addition to your LC tank}
- Frequency of operation $f_0 = 2.4$GHz
- $V_{DD} = 1.2$V
- v_{in} to v_{out} voltage gain ≥ 20dB over at least ±50MHz BW around f_0 {S_{11} < -10dB mandatory}
- NF ≤ 2dB; model $\alpha = 0.85$, $\gamma = 2$, $\delta = 4$ and $|c| = 0.395$ for all devices in the signal path {as shown in the tutorial}
- $IIP_3 \geq$ -6dBm (use two tones separated by 1MHz for your simulations)
- Minimise power consumption (P_{diss})

(b) Now, use ASITIC to design spiral inductors for the values in your design above. Replace the equivalent parallel RLC circuits of part (a) with the parasitic-laden ASITIC π-model (pix command) and compare the LNA performance with that from part (a).{There is no need to optimise either the inductors or LNA in this part – simply achieve Q ≥ 10 for each inductor, plug the models into your netlist and simulate; outer diameter of each inductor ≤ 200µm}

Notes:

1. E-submission only – submit a zip file containing your project report and the Eldo netlist file.
2. Grading will be relative to all four LNA performance metrics: Gain, NF, IIP_3 and P_{diss}. However, note that a design having Gain = 20dB, NF = 2dB, IIP_3 = -6dBm (all exactly on spec) and least P_{diss} is the most preferable situation.
3. Number of inductors: we will assume that your design is normalised to the common-source LNA discussed in class. Therefore, no more than 3 inductors are allowed in your design.
4. Explicitly bias your LNA using a current mirror {i.e. do not use a V_{bias} at the gate}. Also, connect all NMOS bulks to ground. Connecting them locally to the sources is not allowed.
5. Novel circuit topologies may be given bonus points at the discretion of the Instructor.