Lecture # 9 : MOS Device Operation

Long-channel

In linear region:

$$I_D = \mu_n C_{ox} \frac{W}{L}\left[(V_{GS}-V_T)V_{DS} - \frac{V_{DS}^2}{2}\right]$$

for small V_{DS},

$$I_D = \mu_n C_{ox} \frac{W}{L}(V_{GS}-V_T)\cdot V_{DS} \Rightarrow \text{voltage controlled resistor}$$

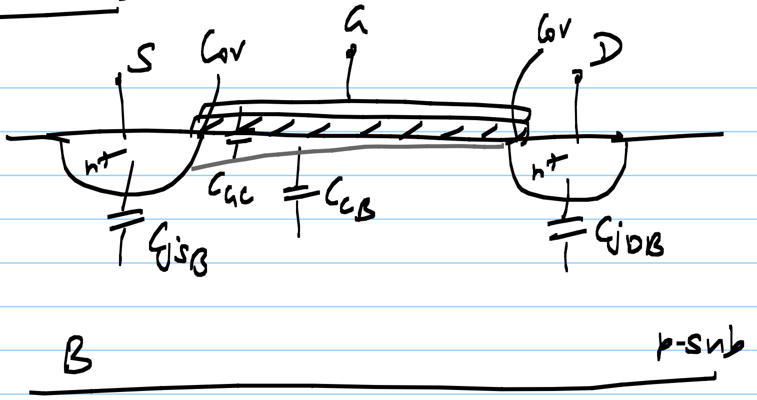
In saturation:

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_T)^2 \quad \text{square law dependence}$$

At "low" frequencies: ignore device caps (e.g. bias)

At "high" frequencies: consider all appropriate device caps.

Capacitances



L_D = overlap of gate over S & D

$L_{eff} = L - 2L_D$

$C_{gc} = C_{ox}\cdot W \cdot L_{eff}$

$C_{cb} = \frac{\epsilon_{si}}{x_d}\cdot W\cdot L_{eff}$

cap	OFF	TRIODE	SAT.
C_{gs}	C_{ov}	$C_{ov} + \frac{C_{gc}}{2}$	$\frac{2}{3}C_{gc} + C_{ov}$
C_{gd}	C_{ov}	$C_{ov} + \frac{W L_{eff} C_{ox}}{2}$	C_{ov}
C_{gb}	$C_{gc} \parallel C_{cb} < C_{gb} < C_{gc}$	0	0
C_{sb}	C_{jsb}	$C_{jsb} + C_{cb}/2$	$C_{jsb} + 2C_{cb}/3$
C_{db}	C_{jdb}	$C_{jdb} + \frac{C_{cb}}{2}$	C_{jdb}

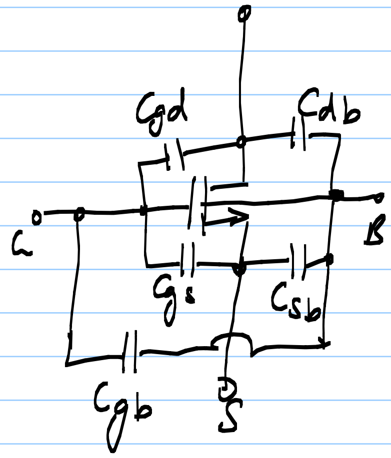
$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$

$C_{ov} = W L_D C_{ox}$

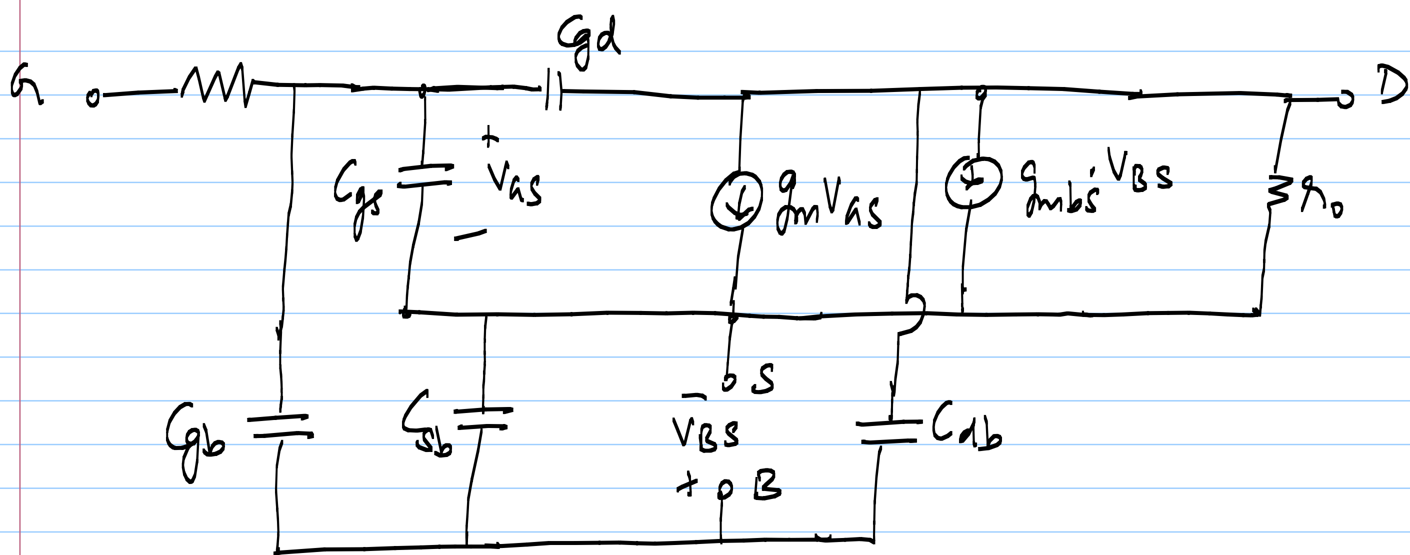
D

$$x_d = \sqrt{\frac{2\epsilon_{si}}{qN_{sub}} \left| \phi_s - \phi_F \right|}$$

{depletion layer depth}



MOSFET MODEL



1) $$g_m = \left.\frac{\partial I_D}{\partial V_{GS}}\right|_{V_{DS}=\text{const.}} = \mu_n C_{ox} \frac{W}{L}(V_{GS} - V_T)$$

$$= \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D}$$

$$= \frac{2 I_D}{V_{GS} - V_T} = \frac{2 I_D}{V_{DSAT.}}$$

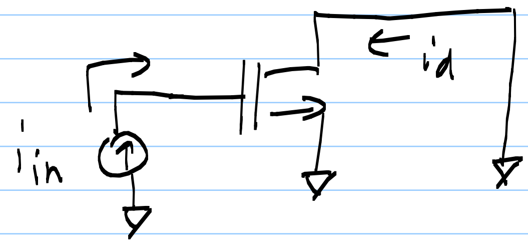
2) $r_o = \dfrac{\partial V_{DS}}{\partial I_D} = \dfrac{1}{\lambda I_D}$

3) $g_{mb} = \dfrac{\partial I_D}{\partial V_{BS}} = \eta\, g_m = \dfrac{\gamma}{2\sqrt{2\Phi_F + V_{SB}}} \cdot g_m$

4) f_T : "Transition Frequency"

$\equiv$ Frequency at which current gain $= 1$

$\omega_T = 2\pi f_T$ is often used



* neglects C_{db}, r_g
* Effect of C_{gd} only on Z_{in} is considered.

$$\left|\frac{i_d}{i_{in}}\right| \approx \frac{g_m}{\omega (C_{gs} + C_{gd})}$$

$$\left|\frac{i_d}{i_{in}}\right| = 1 \quad \text{at} \quad \omega_T = \frac{g_m}{C_{gs} + C_{gd}}$$

$$\left|\frac{i_d}{i_{in}}\right| \approx \frac{\omega_T}{\omega}$$

Long-channel devices:

$$\omega_T \approx \frac{g_m}{C_{gs}} = \frac{\mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T)}{\frac{2}{3} W L C_{ox}}$$

$$= \frac{3}{2} \frac{\mu_n (V_{GS} - V_T)}{L^2} \Rightarrow \omega_T \uparrow \text{ when } \begin{array}{l} * \ V_{DSAT} \uparrow \\ * \ L \downarrow \end{array}$$

5) f_{max} (ω_{max}) $\equiv$ freq. at which power gain becomes 1

It can be shown that

$$g_{out} = g_m \cdot \frac{C_{gd}}{C_{gd}+C_{gs}} = \omega_T \cdot C_{gd}$$

conjugate match @ output implies

$g_L = g_{out}$

i_d is divided equally between load & device g_{out} itself

assume gate resistance of device is r_g

$$P_{in} = \frac{i_{in}^2 \cdot r_g}{2}$$

$$P_L = \frac{1}{2}\left(i_d/2\right)^2 \cdot g_L$$

$$= \frac{1}{2}\left(\frac{\omega_T}{\omega} i_{in} \cdot \frac{1}{2}\right)^2 \cdot \frac{1}{\omega_T C_{gd}}$$

$$\Rightarrow \frac{P_L}{P_{in}} = \frac{\omega_T}{\omega^2 4 r_g C_{gd}}$$

$$\boxed{\omega_{max} = \frac{1}{2}\sqrt{\frac{\omega_T}{r_g C_{gd}}}}$$

6) <u>NQS effects</u>: consider transit time effects (non-quasi static effects)

$$g_g = \frac{\omega^2 C_{gs}^2}{5 g_{d0}} \approx \frac{g_m}{5}\left(\frac{\omega}{\omega_T}\right)^2$$ $\leftarrow$ this impedance is seen @ gate

Brief note on CMOS "Constant Field Scaling"

1) Reduce all lateral & vertical dimensions by α (>1) $\Rightarrow$ W, L, t_{ox}, depth & perimeter of S, D junctions

2) Reduce V_{DD}s and V_Ts by α

3) Increase all doping levels by α

(1) & (2) $\Rightarrow$ Electric fields stay constant inside the semiconductor

Impact on device parameters:

1) Device current: $I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T)^2$

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} \Rightarrow C_{ox,\alpha} = \frac{\epsilon_{ox}}{t_{ox}/\alpha} = \alpha \cdot C_{ox}$$

$$I_{D,\alpha} = \frac{1}{2} \mu_n (\alpha C_{ox}) \cdot \frac{W/\alpha}{L/\alpha} \left(\frac{V_{GS}}{\alpha} - \frac{V_T}{\alpha} \right)^2$$

$$= I_D \cdot \frac{1}{\alpha}$$

2) Capacitances:

channel cap $\quad C_{ch} = W L C_{ox}$

$$C_{ch,\alpha} = \frac{W}{\alpha} \cdot \frac{L}{\alpha} (\alpha C_{ox}) = C_{ch} \cdot \frac{1}{\alpha}$$

Depl. region width $\quad W_d = \sqrt{\frac{2 \epsilon_{Si}}{q} \left(\frac{1}{N_A} + \frac{1}{N_D} \right) (\phi_B + V_R)}$

$\phi_B = V_T \ln \left(\frac{N_A N_D}{n_i^2} \right)$, V_R = reverse bias voltage assuming $V_R >> \phi_B$,

$$W_{d,\alpha} \approx \sqrt{\frac{2\epsilon_{si}}{q}\left(\frac{1}{\alpha N_A} + \frac{1}{\alpha N_D}\right) \cdot \frac{V_R}{\alpha}}$$

$$= W_d \cdot \frac{1}{\alpha}$$

$\Rightarrow C_{depl,\alpha} = \alpha \cdot C_{depl}$

* in general, all caps $\downarrow$ by a factor of $\frac{1}{\alpha}$

3) Gate delay (CMOS inverter)

$$T_d = \frac{C}{I} \cdot V_{DD}$$

$$T_{d,\alpha} = \frac{C/\alpha}{I/\alpha} \cdot \frac{V_{DD}}{\alpha} = T_d \cdot \frac{1}{\alpha}$$

4) Power consumption (digital)

$$P = f\, C\, V_{DD}^2$$

$$P_\alpha = f \cdot \frac{C}{\alpha} \cdot \left(\frac{V_{DD}}{\alpha}\right)^2 = P \cdot \frac{1}{\alpha^3}$$

5) Layout Density:

$$area_\alpha = \frac{1}{\alpha^2}(area)$$

6) Transconductance:

$$g_m = \mu C_{ox} \frac{W}{L}(V_{GS} - V_T)$$

$$g_{m,\alpha} = \mu(\alpha C_{ox}) \cdot \frac{W/\alpha}{L/\alpha} \cdot \frac{V_{GS} - V_T}{\alpha}$$

$$= g_m$$

Short-channel MOS operation

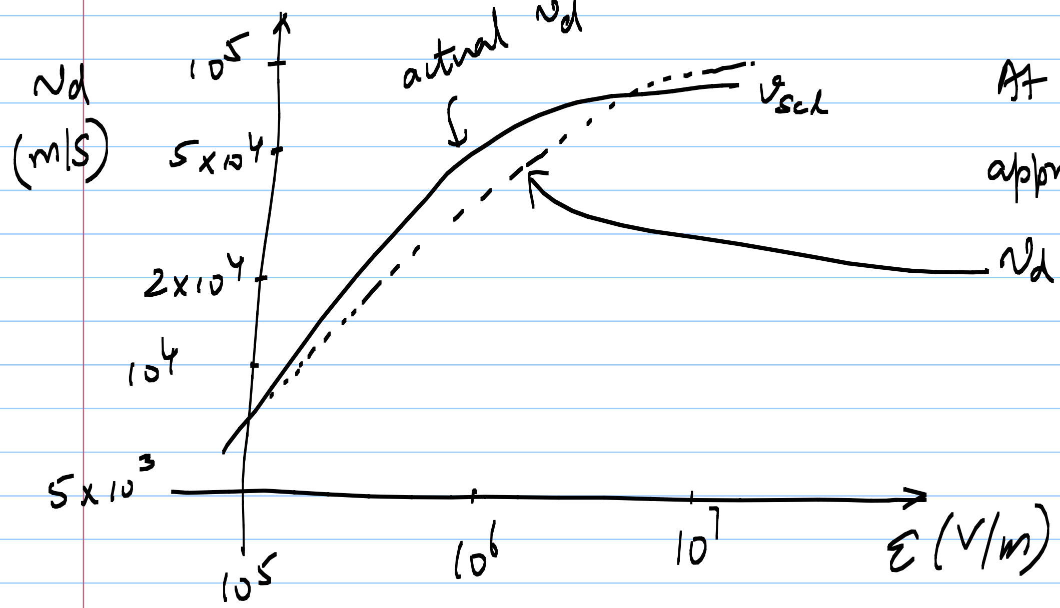
$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_T)^2$$

$\Rightarrow$ Derived using $v_d(y) = \mu_n \mathcal{E}(y)$

drift velocity

horizontal electric field

length along channel



At high fields, an approximate relation is:

$$v_d = \frac{\mu_n \mathcal{E}}{1+\mathcal{E}/\mathcal{E}_c}$$

scattering limited velocity:

$v_{scl} = \mu_n \mathcal{E}_c$

$\mathcal{E}_c \approx 1.5\times10^6$ V/m

$\mu_n \approx 0.07\,m^2/Vs$

long-channel device in sat.:

$$I_D = \frac{\mu_n C_{ox}}{2}\cdot\frac{W}{L}(V_{GS}-V_T)\cdot V_{DSAT}$$

$$V_{DSAT}\text{(long ch.)} = (V_{GS}-V_T)$$

In general,

$$V_{DSAT} = (V_{GS}-V_T)\,\|\,(L\cdot\mathcal{E}_c)$$

$$= \frac{(V_{GS}-V_T)(L\mathcal{E}_c)}{(V_{GS}-V_T)+(L\mathcal{E}_c)}$$

$$I_D = \frac{\mu_n C_{ox}}{2} \frac{W}{L} (V_{GS}-V_T)\left[(V_{GS}-V_T) \,||\, (L\cdot \mathcal{E}_c)\right]$$

prominence of short channel effects

$\Rightarrow$ compare $\frac{V_{GS}-V_T}{L}$ and $\mathcal{E}_c$ (ratio)

If small $\Rightarrow$ long channel approx. is valid

(actual length of gate is irrelevant)

* as L decreases, smaller $(V_{GS}-V_T)$ is needed to exhibit short-channel effects!

Rewrite:

$$I_D = W C_{ox} (V_{GS}-V_T) \cdot v_{sat} \left[1 + \frac{L\,\mathcal{E}_c}{V_{GS}-V_T}\right]^{-1}$$

In deep velocity saturation,

$$I_D = \frac{\mu_n C_{ox}}{2} \frac{W}{L} (V_{GS}-V_T) \left[L\cdot \mathcal{E}_c\right]$$

$$= \frac{\mu_n C_{ox}}{2} \cdot W \, (V_{GS}-V_T) \cdot \mathcal{E}_c$$

$\Rightarrow$ Drain current independent of L!

$\Rightarrow$ $I_D - V_{GS}$ relationship is linear!

* $g_m = \frac{\partial I_D}{\partial V_{GS}} = \frac{\mu_n C_{ox}}{2} \cdot W \cdot \mathcal{E}_c$

* $C_{gs} = \frac{2}{3} W L C_{ox}$

* $\omega_T = \frac{g_m}{C_{gs}} = \frac{3}{4} \frac{\mu_n \mathcal{E}_c}{L}$

$\Rightarrow \omega_T \propto \frac{1}{L}$ [was $\frac{1}{L^2}$ for long-channel]

$\Rightarrow \omega_T$ does not depend on bias conditions (as long as device is in sat.), or oxide thickness (t_{ox}, C_{ox})

* PMOS devices show saturation effects at higher fields (holes vs e^-s)