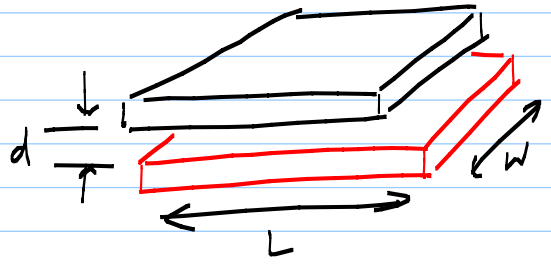
Lecture #8: Capacitors, Varactors

Linear caps

* Special RF processes - metal-insulator-metal (MIM) capacitors - use special high-k dielectrics (denser caps) — costly
* Standard processes - MOM caps (oxide)

problem: Oxide thickness is normally large to reduce cap. between layers - cap/unit area (~ 0.1-0.2 fF/μm^2)

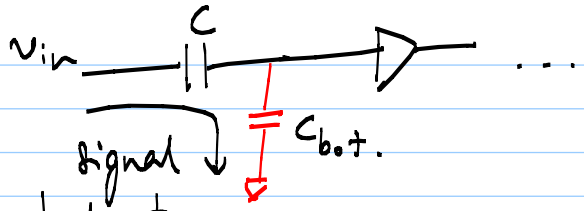


$$C \simeq \epsilon \frac{W \cdot L}{d}$$

d = thickness of oxide between metal layers

* another issue: bottom-plate cap. (to lower metal or substrate)

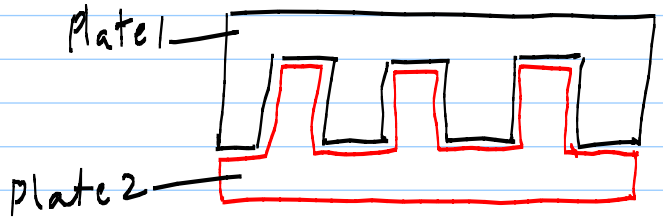
⇒ can be as high as 10-30% of cap



* Be careful how you design ac coupling caps!

* Fringing can be significant for caps with small W, L
* Temperature coefficient is often small

lateral flux capacitor

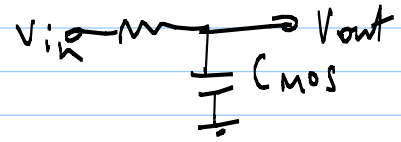


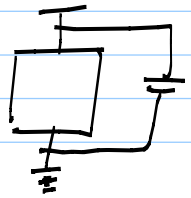
* better density
* can use multiple layers to increase density
* min. metal-metal spacing decreases with process scaling

* parasitic bottom plate cap is smaller (because of better density)
* lateral cap depends on perimeter
  ⇒ use layouts that maximise perimeter (e.g. fractals)

MOS capacitor

* gate capacitance of MOSFET ~ 1-2 fF/μm width
* larger temp-co (depends on doping levels)
* single-ended caps – can be used for grounded caps (e.g. supply bypass, single-ended filtering etc.)

a) 

b) 

* $C_{MOS} = f(V)$
  ⇒ small-signal cases only
  ⇒ DC bias is critical

Varactor ⇒ device whose capacitance can be varied using a voltage (≡ voltage controlled capacitance)

* can be used to tune a resonant circuit, and hence a receiver/transmitter

remember: For a reverse-biased p-n junction

$$C_{var} = \frac{C_0}{\left(1 + \frac{V_R}{\phi_B}\right)^m}$$

ϕ_B = Built-in potential of junction

$m = 0.5$ for an abrupt junction

$m \sim 0.3 - 0.4$ for typical CMOS processes

thickness of depletion region changes with V_R

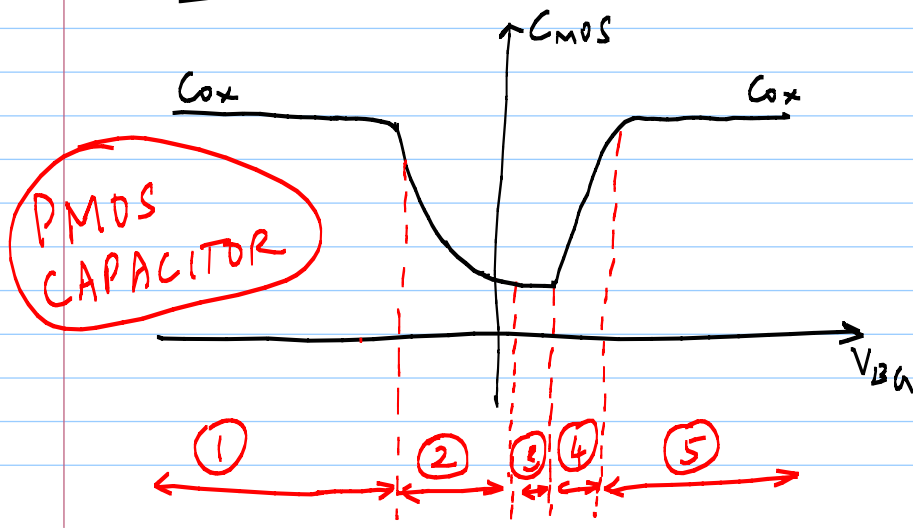
Varactor diodes: diodes whose junctions are graded to a) Control $C = f(V_R)$ [linear, quadratic etc.]

b) maximise $\frac{C_{max}}{C_{min}}$ (i.e. maximise tuning range)

* Symbol: 

* not so common in CMOS processes nowadays

MOS Varactors



1 : Accumulation

2 : Depletion

3 : Weak Inversion

4 : Moderate Inversion

5 : Strong Inversion

$V_{BG} \geq |V_T|$ ⇒ strong inversion (transistor behaviour)

$V_{BG} << 0$ ⇒ accumulation

(i.e. $V_G >> V_B$) gate oxide–substrate interface allows electrons to flow freely (Interface Voltage > 0)

In both conditions, $C_{MOS} = C_{ox}$ (across gate oxide)

In depletion, weak and moderate inversion

→ very few (mobile) charge carriers @ oxide–substrate interface

→ $C_{MOS} < C_{ox}$

* In strong inversion,

$$R_{MOS} \approx \frac{L}{12 K_p W (V_{BG} - |V_T|)}$$

{not valid @ $V_{BG} = |V_T|$}

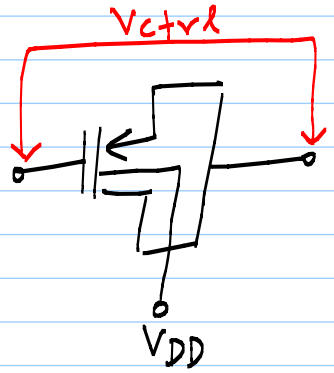
* C_{MOS} vs. V_{BA} is non-monotonic

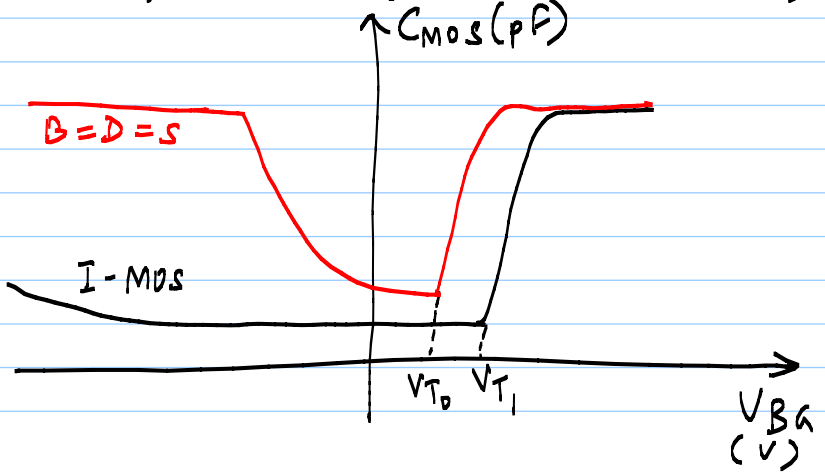
→ not good for tuning!

1) Inversion-mode varactors

→ Prevent transistor from enter accumulation region

* disconnect D-S from B
* connect B to highest voltage available (ie. V_{DD})



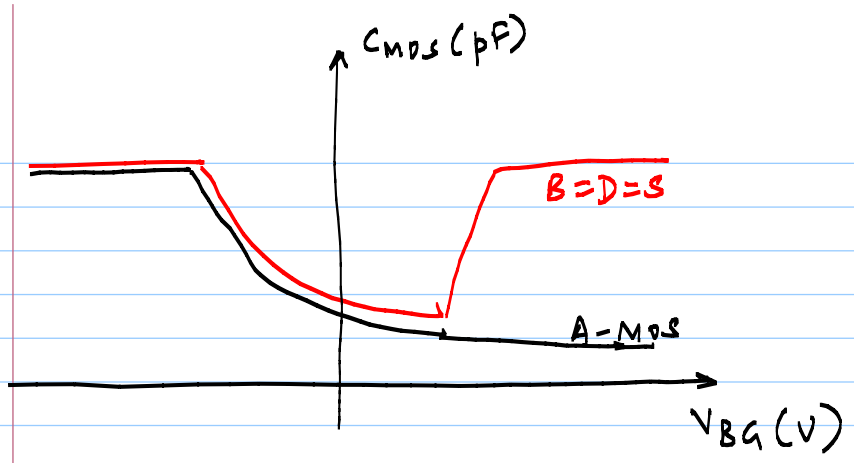


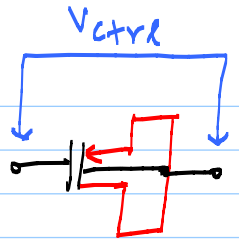
* $V_{T_1} > V_{T_0}$ due to substrate effect ($V_B > V_S$)
* tuning range of I-MOS is much wider
* NMOS cap shows similar effect
  → lower R_{MOS} due to $\mu_n > \mu_p$
  → more sensitive to substrate noise
  (PMOS is in an n-well)

2) Accumulation mode varactors

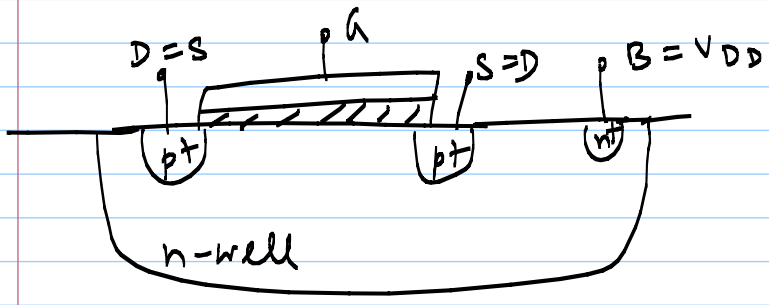
→ Inhibit formation of inversion layer

* remove D-S pt diffusions
* Place bulk contacts to reduce parasitic n-well resistance
* No extra process steps required; however A-MOS device may not be characterised/modelled

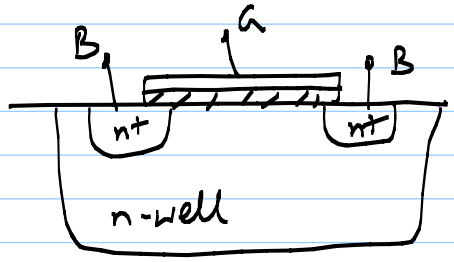




I-Mode



A-Mode



* $Q_{I\text{-}MOS} > Q_{A\text{-}MOS}$
* nMOS varactor shows better Q
* Gate node is usually connected to signal
  - higher Q
  - lower parasitic cap
* $\frac{C_{max}}{C_{min}}$ is limited by C_{GD} & C_{GS} overlap caps (i.e. C_{min})
* high Q ⇒ minimum L (R_{MOS} is lower)
  high $\frac{C_{max}}{C_{min}}$ ⇒ large L (overlap fraction is lower)
  } basic varactor tradeoff
* $C_{MOS} - V_{BG}$ characteristics are for small-signal applied around DC V_{BG}; If signal is large (e.g. VCO), instantaneous value of C_{MOS} changes

through signal period.

→ average $C_{MOS} = f(V_{BA})$

→ monotonicity is very important

* Varactor Qs are usually much higher (20-40) than inductor Qs (5-10)

* Varactor Diode C_{max}/C_{min} can be increased by biasing the diode closer to forward-biasing

→ However, Q drops very quickly

→ large signal conditions may forward bias the diode