Lecture #7: RF inductors, Transformers (cont'd.)

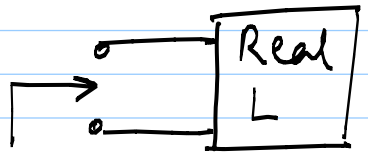
Figures of Merit:

1) Q: usually want this to be maximised in the frequency range of interest
   - note that the model is not a simple series or parallel RLC

how is Q determined?

a) Physical definition: $2\pi \cdot \frac{E_{stored(peak)}}{E_{loss\ per\ cycle}}$

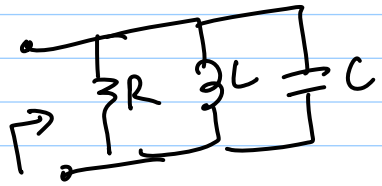
b)



$$Z_{in} = \frac{1}{Y_{in}}$$

$$Q = \frac{Im(Z_{in})}{Re(Z_{in})} = \frac{Im(Y_{in})}{Re(Y_{in})}$$

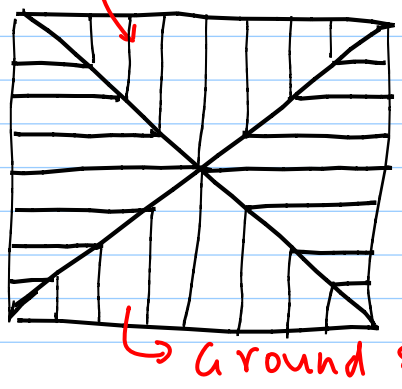
$$Q = f(L_s, R_s, C_c, C_{ox}, C_{si}, R_{si})$$



$$Q_{ind} = \frac{\frac{1}{\omega L} - \omega C}{\frac{1}{R}}$$

{ in inductive region }

* SOI processes show much higher Q than regular CMOS processes
* Substrate losses reduce with distance from substrate – Use highest possible metal (these are also usually thicker than lower metals)
* Use Patterned ground Shield, if appropriate
  - better Q : a) current loops are broken by slotting – eddy currents ↓



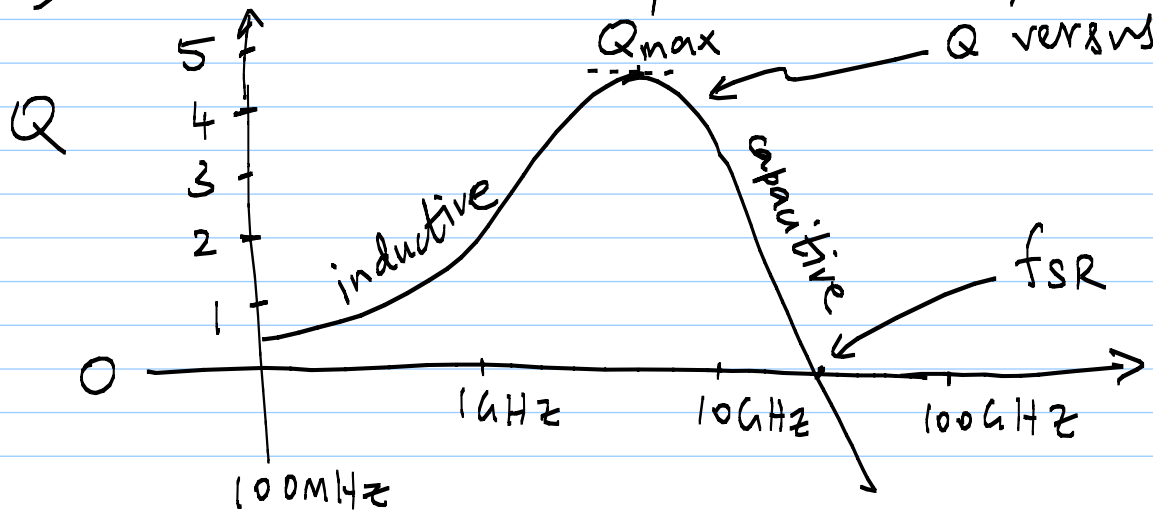
  - also reduces substrate noise coupling
  - more shunt capacitance (shield is now closer than substrate)

2) Self-resonant frequency fsr
  - Frequency at which inductance of spiral resonates with its own capacitive parasitics

* Real inductors have capacitive parasitics
* Real capacitors have inductive parasitics
* Remember – tank circuits have both inductors & capacitors
* Patterned ground shield reduces fsr

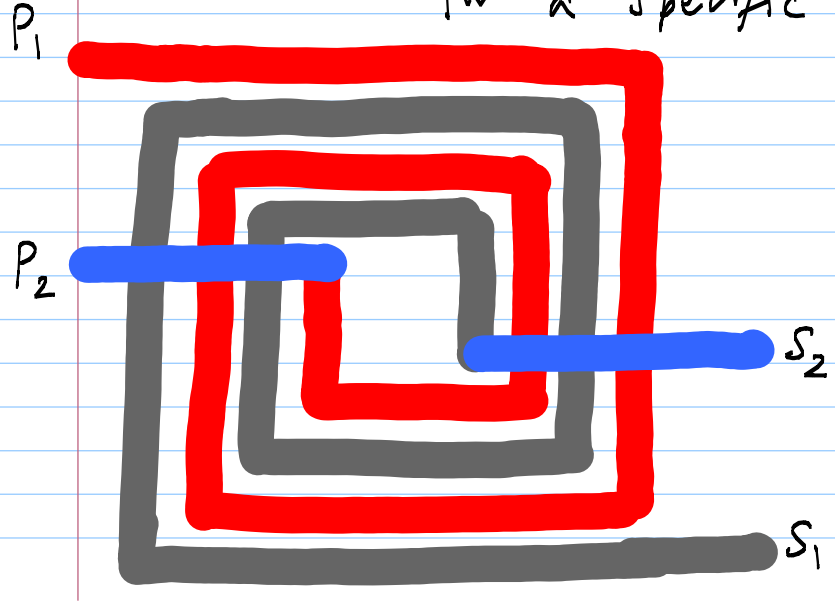
- at f_{SR}, inductor impedance is purely resistive, and $Q_{ind} = 0$
- Beyond f_{SR}, the inductor behaves capacitively
- f_{SR} depends on spiral area

3) Total area occupied on chip A



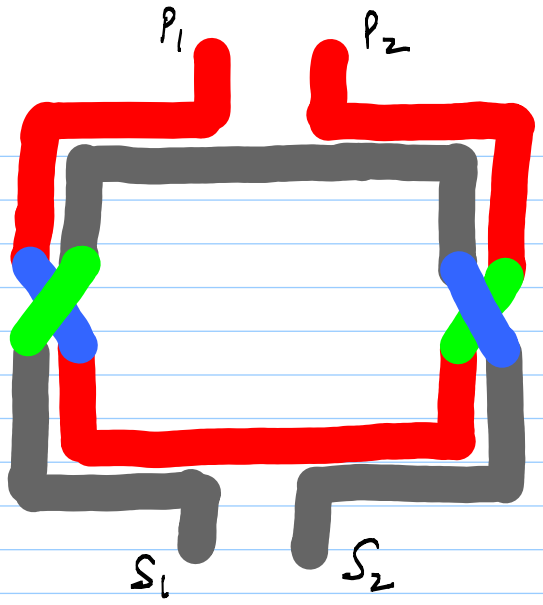
Transformers:

* Used in differential circuits (usually)
* Need to be symmetric
* Coupling factor to be maximised (usually)
  - there are cases where you would design for a specific coupling factor



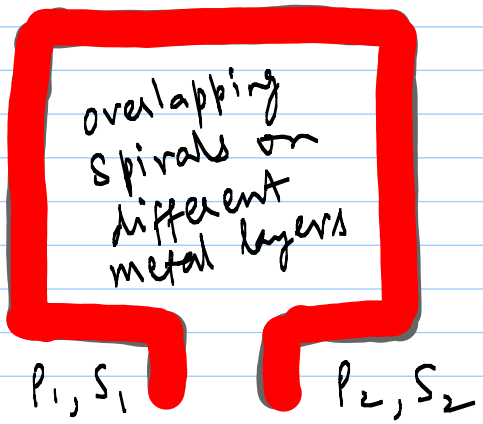
Planar Transformer - 1

* Sideways coupling, n = 2
* Primary & secondary are symmetric
* Ports P_1 & P_2 (S_1 & S_2) are not symmetric



Planar Transformer – 2

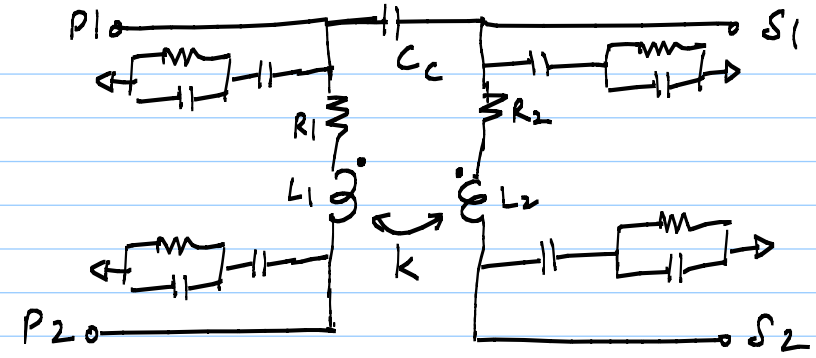
* n = 1
* P & S symmetric
* $P_1 - P_2$ & $S_1 - S_2$ are more symmetric than case 1
  – underpass causes asymmetry



Vertical Transformer

* n = 1
* P & S are completely asymmetric (different metal layers)

Transformer π-model



* Can cascade coils on multiple metal layers to make a spiral with large L in a given area
  – larger series resistance due to higher R of lower metal layers
  – useful to create "RF chokes" for PAs and wideband RF amplifiers

Other things to remember

* Overall LC tank Q is often limited by inductor Q
* Don't place anything close to a spiral (ind. or xfmr.)
* Use a guard ring around inductor for noise isolation and to provide good EM boundary conditions
* No metal fill inside/ inductor (what is this?)
* maintain symmetry - gives higher Q
* Via resistance matters - use lots of vias in parallel if you need to change metal layers

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Note: * Project 1 will involve spiral inductor design using ASITIC

* You will be designing your own inductors using ASITIC for projects 2, 3 & 4 also. The design of the inductor <u>will</u> impact circuit performance, so learn this well.
* HW2 will include an impedance matching problem with a <u>real</u> inductor.